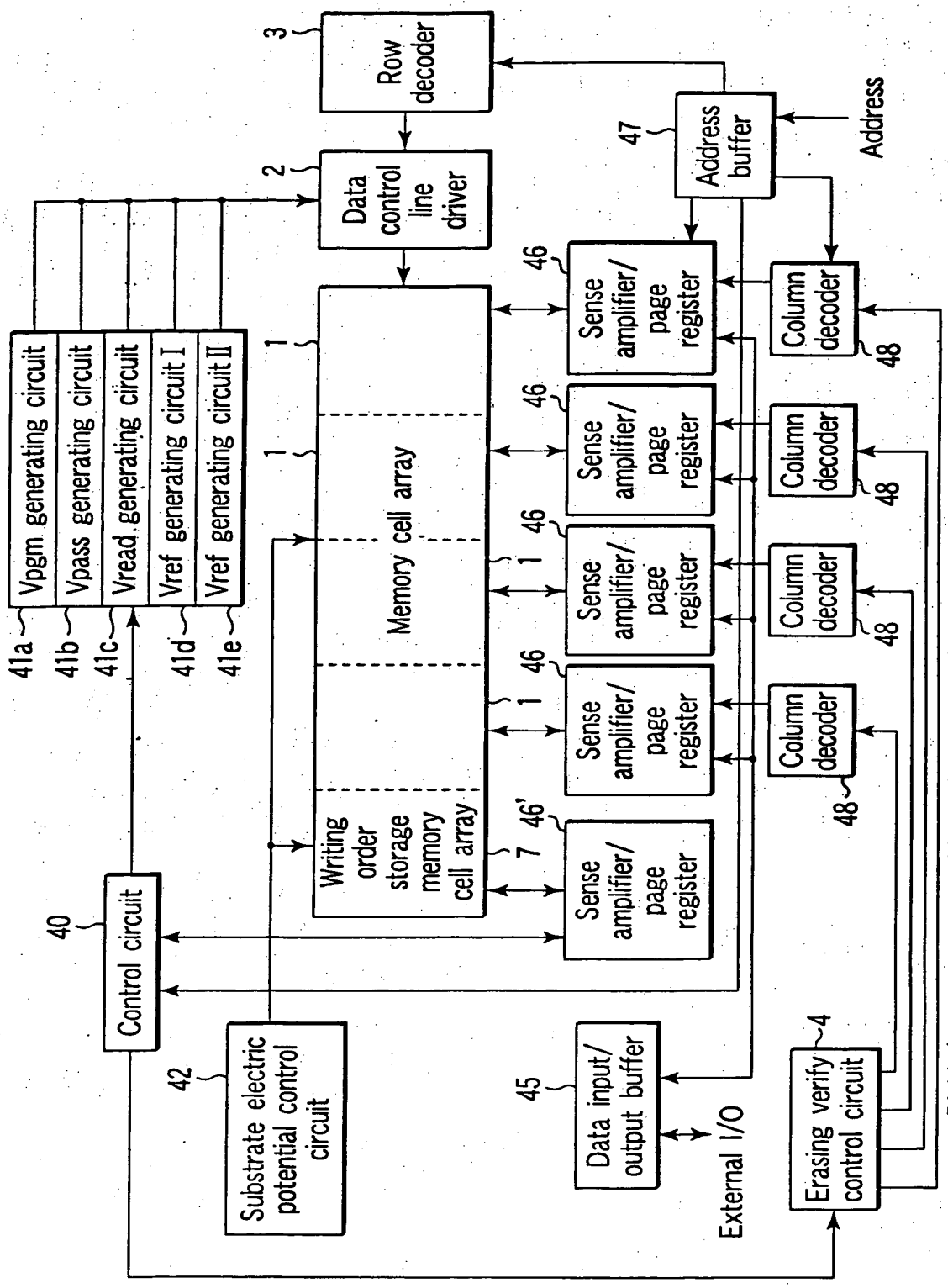
Row decoder
Data control line driver
Address buffer
Address
Vpgm generating circuit
Vpass generating circuit
Vread generating circuit
Vref generating circuit I
Vref generating circuit II
41a
41b
41c
41d
41e
Memory cell array
Writing order storage memory cell array
Sense amplifier/ page register
Column decoder
Control circuit
Substrate electric potential control circuit
Data input/ output buffer
External I/O
Erasing verify control circuit
Divided page sense amplifier selective signal

FIG. 1

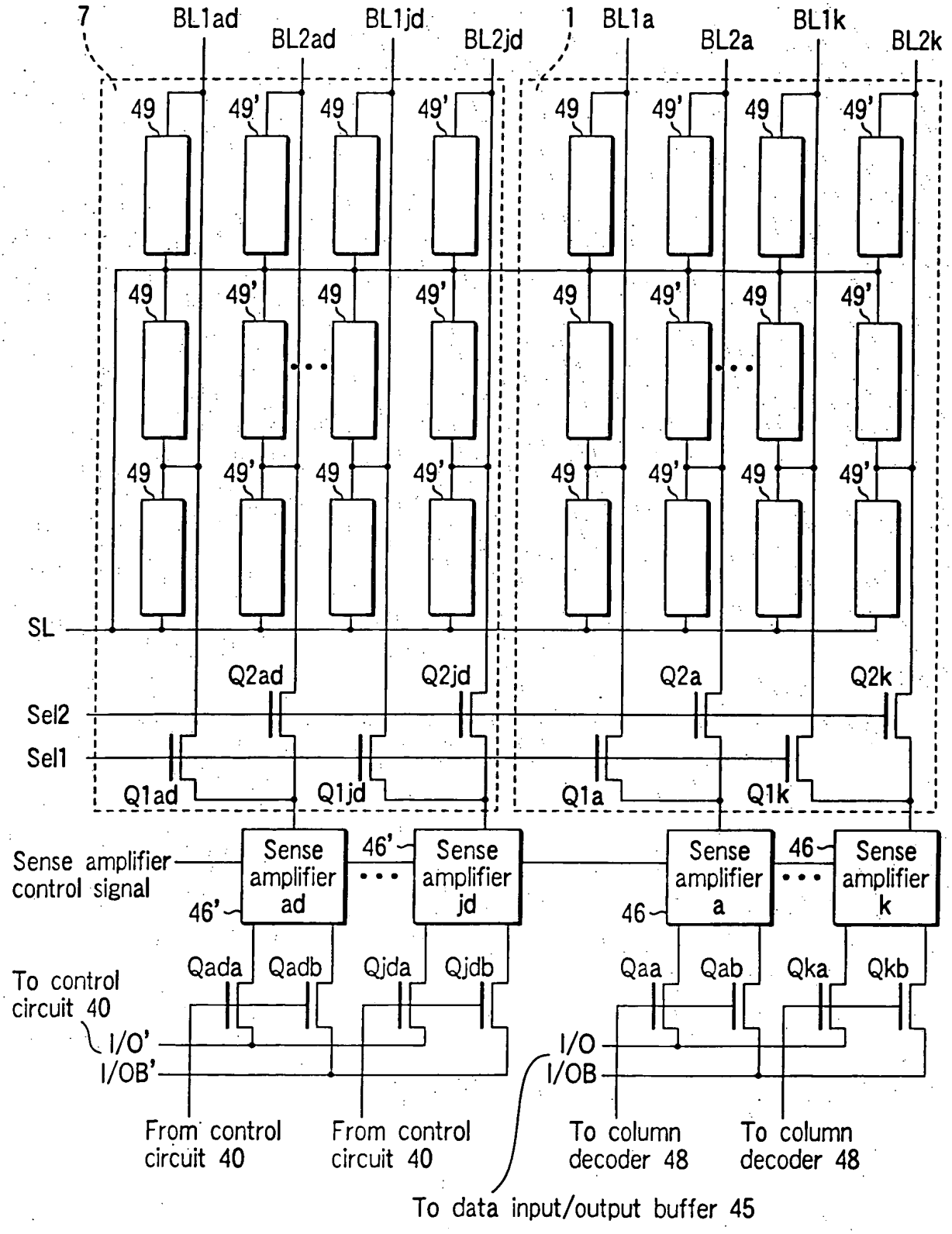
7
BL1ad
BL2ad
BL1jd
BL2jd
1
BL1a
BL2a
BL1k
BL2k
49
49'
SL
Sel2
Sel1
Q2ad
Q2jd
Q2a
Q2k
Q1ad
Q1jd
Q1a
Q1k
Sense amplifier control signal
Sense amplifier ad
Sense amplifier jd
Sense amplifier a
Sense amplifier k
46
46'
Qada
Qadb
Qjda
Qjdb
Qaa
Qab
Qka
Qkb
To control circuit 40
I/O'
I/OB'
I/O
I/OB
From control circuit 40
From control circuit 40
To column decoder 48
To column decoder 48
To data input/output buffer 45

FIG. 2

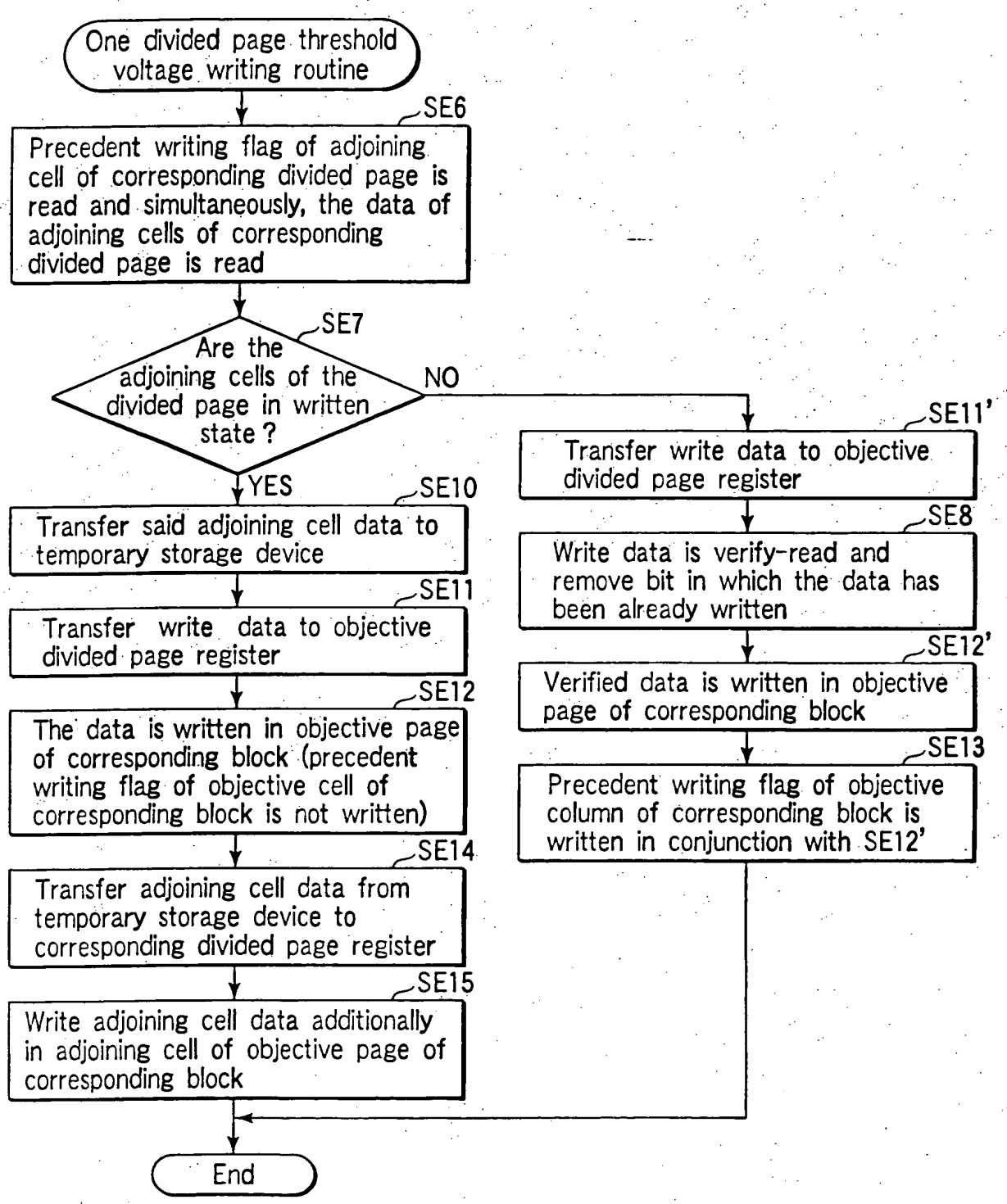
One divided page threshold voltage writing routine
SE6
Precedent writing flag of adjoining cell of corresponding divided page is read and simultaneously, the data of adjoining cells of corresponding divided page is read
SE7
Are the adjoining cells of the divided page in written state ?
NO
YES
SE10
Transfer said adjoining cell data to temporary storage device
SE11
Transfer write data to objective divided page register
SE12
The data is written in objective page of corresponding block (precedent writing flag of objective cell of corresponding block is not written)
SE14
Transfer adjoining cell data from temporary storage device to corresponding divided page register
SE15
Write adjoining cell data additionally in adjoining cell of objective page of corresponding block
SE11'
Transfer write data to objective divided page register
SE8
Write data is verify-read and remove bit in which the data has been already written
SE12'
Verified data is written in objective page of corresponding block
SE13
Precedent writing flag of objective column of corresponding block is written in conjunction with SE12'
End

FIG. 3

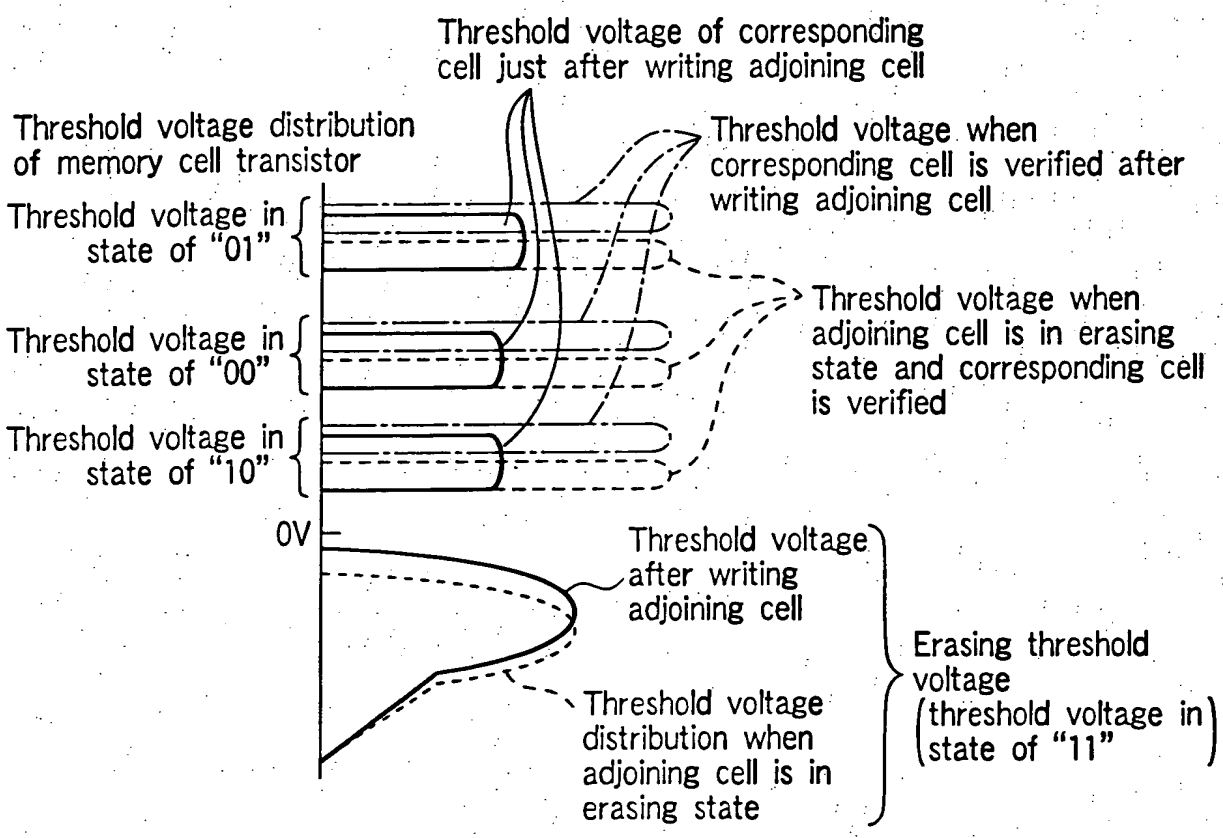
Threshold voltage of corresponding cell just after writing adjoining cell
Threshold voltage distribution of memory cell transistor
Threshold voltage when corresponding cell is verified after writing adjoining cell
Threshold voltage in state of "01"
Threshold voltage when adjoining cell is in erasing state and corresponding cell is verified
Threshold voltage in state of "00"
Threshold voltage in state of "10"
0V
Threshold voltage after writing adjoining cell
Threshold voltage distribution when adjoining cell is in erasing state
Erasing threshold voltage (threshold voltage in state of "11")

FIG. 4

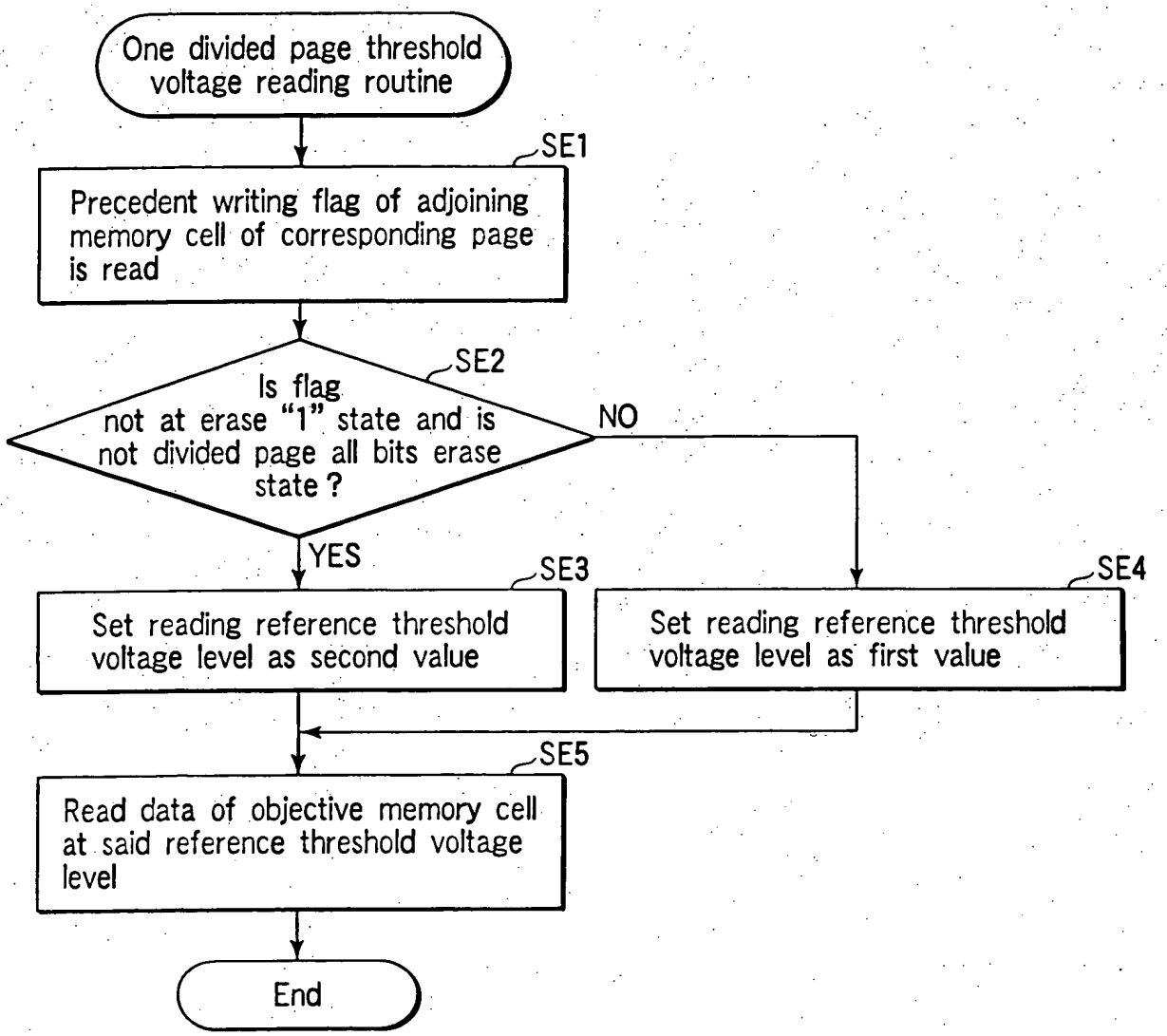
One divided page threshold voltage reading routine
SE1
Precedent writing flag of adjoining memory cell of corresponding page is read
SE2
Is flag not at erase "1" state and is not divided page all bits erase state ?
NO
YES
SE3
Set reading reference threshold voltage level as second value
SE4
Set reading reference threshold voltage level as first value
SE5
Read data of objective memory cell at said reference threshold voltage level
End

FIG. 5

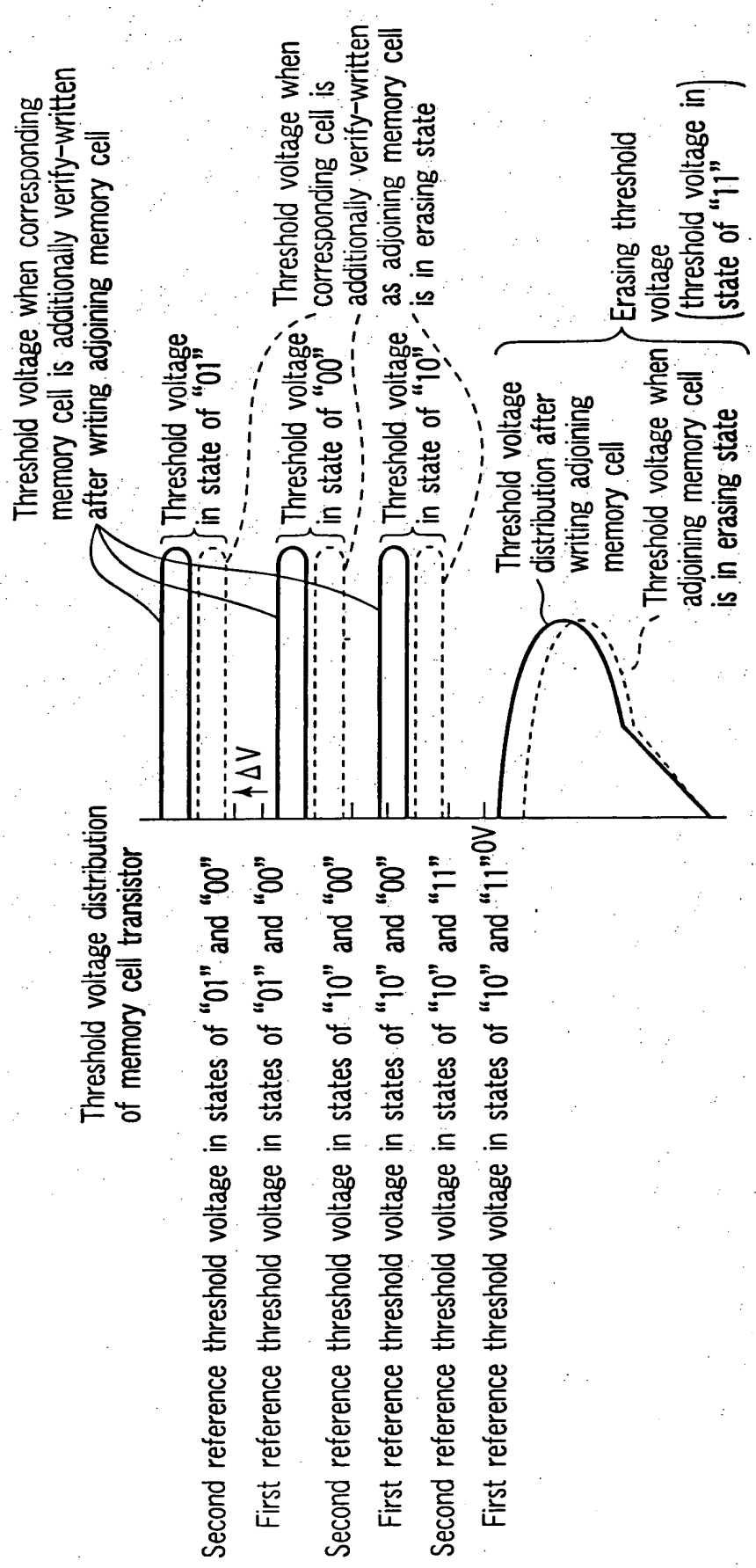
Threshold voltage distribution of memory cell transistor
Threshold voltage when corresponding memory cell is additionally verify-written after writing adjoining memory cell
Threshold voltage in state of "01"
Threshold voltage when corresponding cell is additionally verify-written as adjoining memory cell is in erasing state
Threshold voltage in state of "00"
Threshold voltage in state of "10"
ΔV
Second reference threshold voltage in states of "01" and "00"
First reference threshold voltage in states of "01" and "00"
Second reference threshold voltage in states of "10" and "00"
First reference threshold voltage in states of "10" and "00"
Second reference threshold voltage in states of "10" and "11"
First reference threshold voltage in states of "10" and "11"
0V
Threshold voltage distribution after writing adjoining memory cell
Threshold voltage when adjoining memory cell is in erasing state
Erasing threshold voltage (threshold voltage in state of "11")

FIG. 6

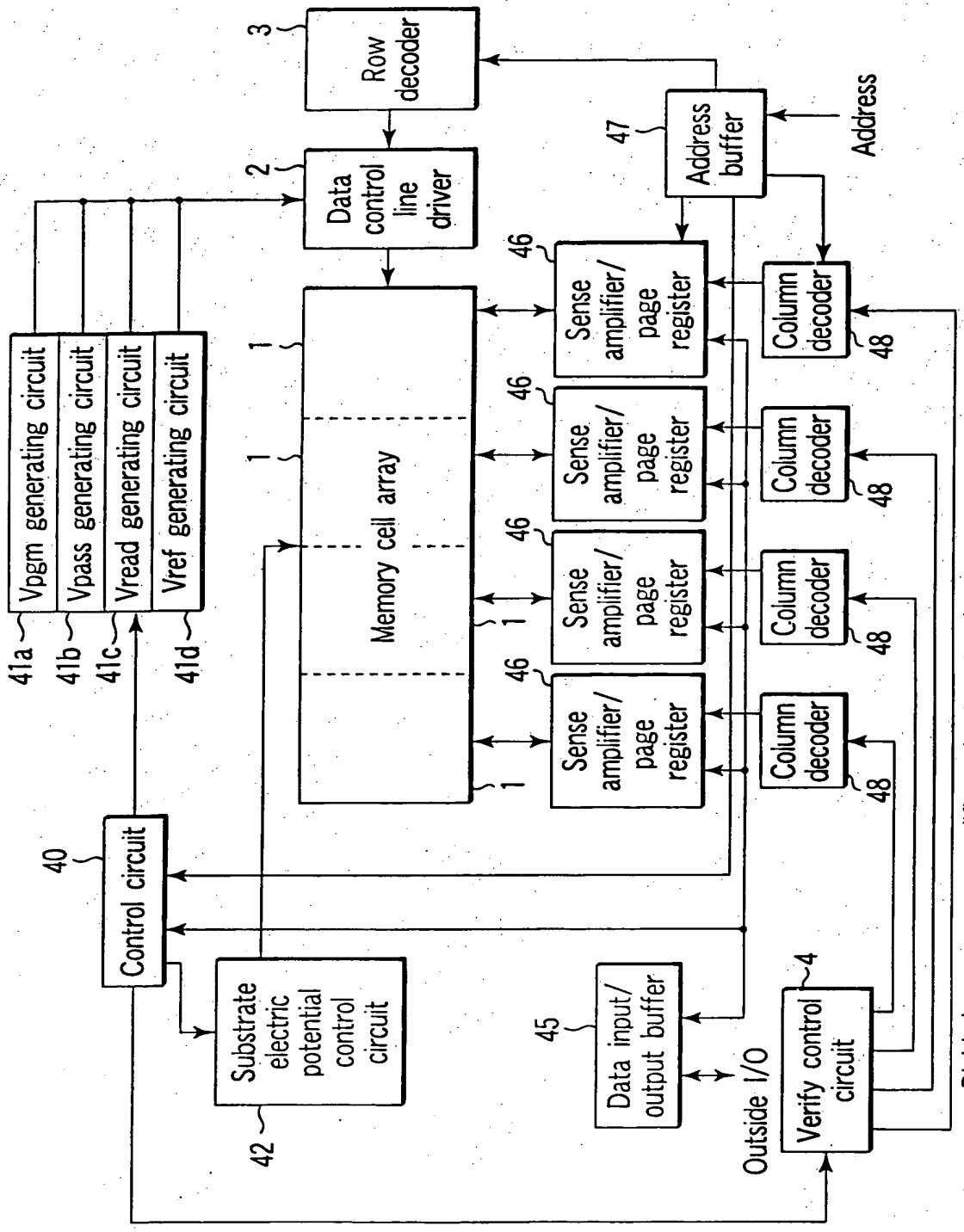
Row decoder
Data control line driver
Address buffer
Address
Memory cell array
Sense amplifier/ page register
Column decoder
Vpgm generating circuit
Vpass generating circuit
Vread generating circuit
Vref generating circuit
Control circuit
Substrate electric potential control circuit
Data input/ output buffer
Outside I/O
Verify control circuit
Divided page sense amplifier selective signal

FIG. 7

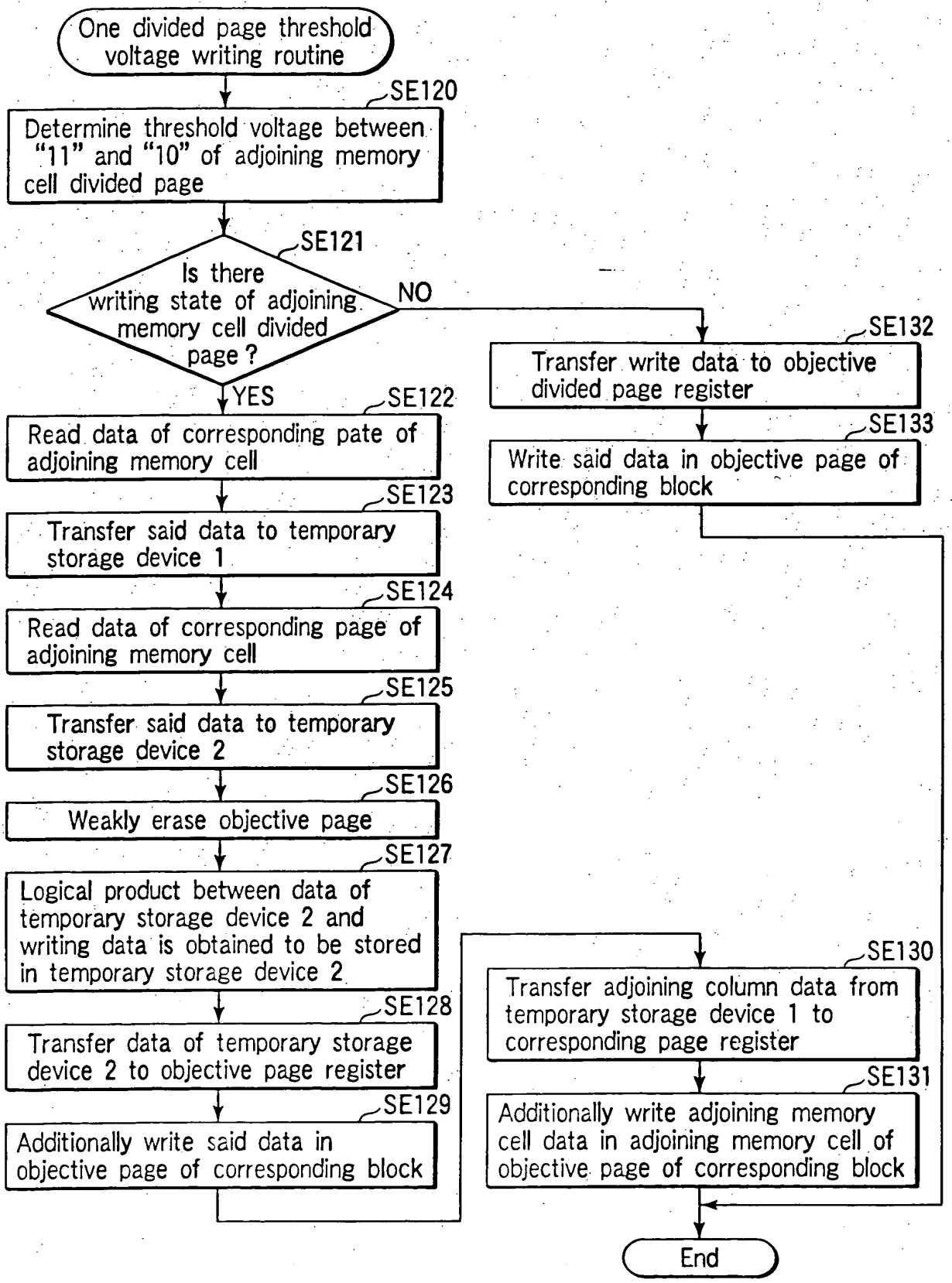
One divided page threshold voltage writing routine
SE120
Determine threshold voltage between "11" and "10" of adjoining memory cell divided page
SE121
Is there writing state of adjoining memory cell divided page ?
NO
YES
SE122
Read data of corresponding pate of adjoining memory cell
SE123
Transfer said data to temporary storage device 1
SE124
Read data of corresponding page of adjoining memory cell
SE125
Transfer said data to temporary storage device 2
SE126
Weakly erase objective page
SE127
Logical product between data of temporary storage device 2 and writing data is obtained to be stored in temporary storage device 2
SE128
Transfer data of temporary storage device 2 to objective page register
SE129
Additionally write said data in objective page of corresponding block
SE132
Transfer write data to objective divided page register
SE133
Write said data in objective page of corresponding block
SE130
Transfer adjoining column data from temporary storage device 1 to corresponding page register
SE131
Additionally write adjoining memory cell data in adjoining memory cell of objective page of corresponding block
End

FIG. 8

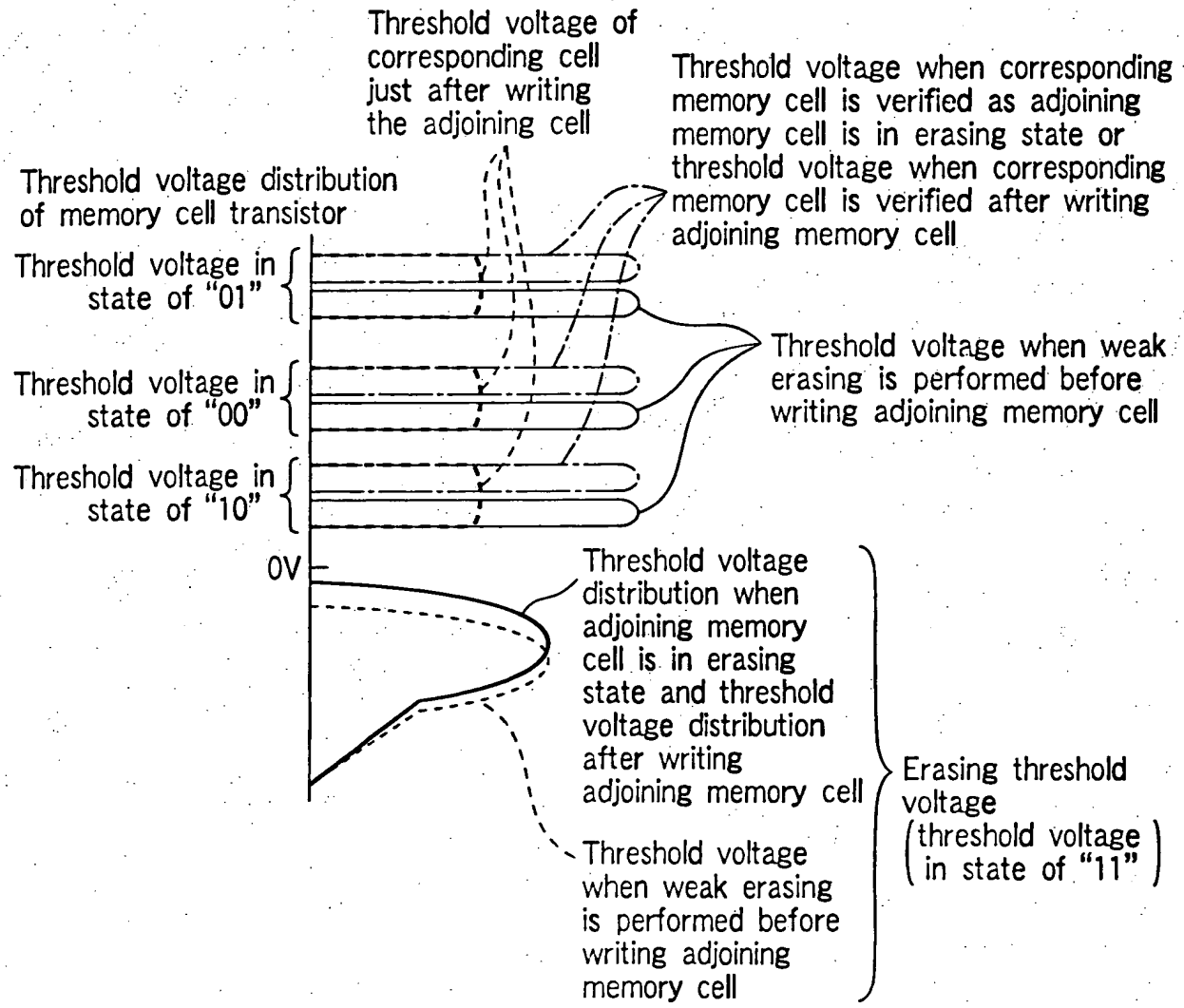
Threshold voltage of corresponding cell just after writing the adjoining cell
Threshold voltage when corresponding memory cell is verified as adjoining memory cell is in erasing state or threshold voltage when corresponding memory cell is verified after writing adjoining memory cell
Threshold voltage distribution of memory cell transistor
Threshold voltage in state of "01"
Threshold voltage in state of "00"
Threshold voltage in state of "10"
Threshold voltage when weak erasing is performed before writing adjoining memory cell
0V
Threshold voltage distribution when adjoining memory cell is in erasing state and threshold voltage distribution after writing adjoining memory cell
Threshold voltage when weak erasing is performed before writing adjoining memory cell
Erasing threshold voltage (threshold voltage in state of "11")

FIG. 9

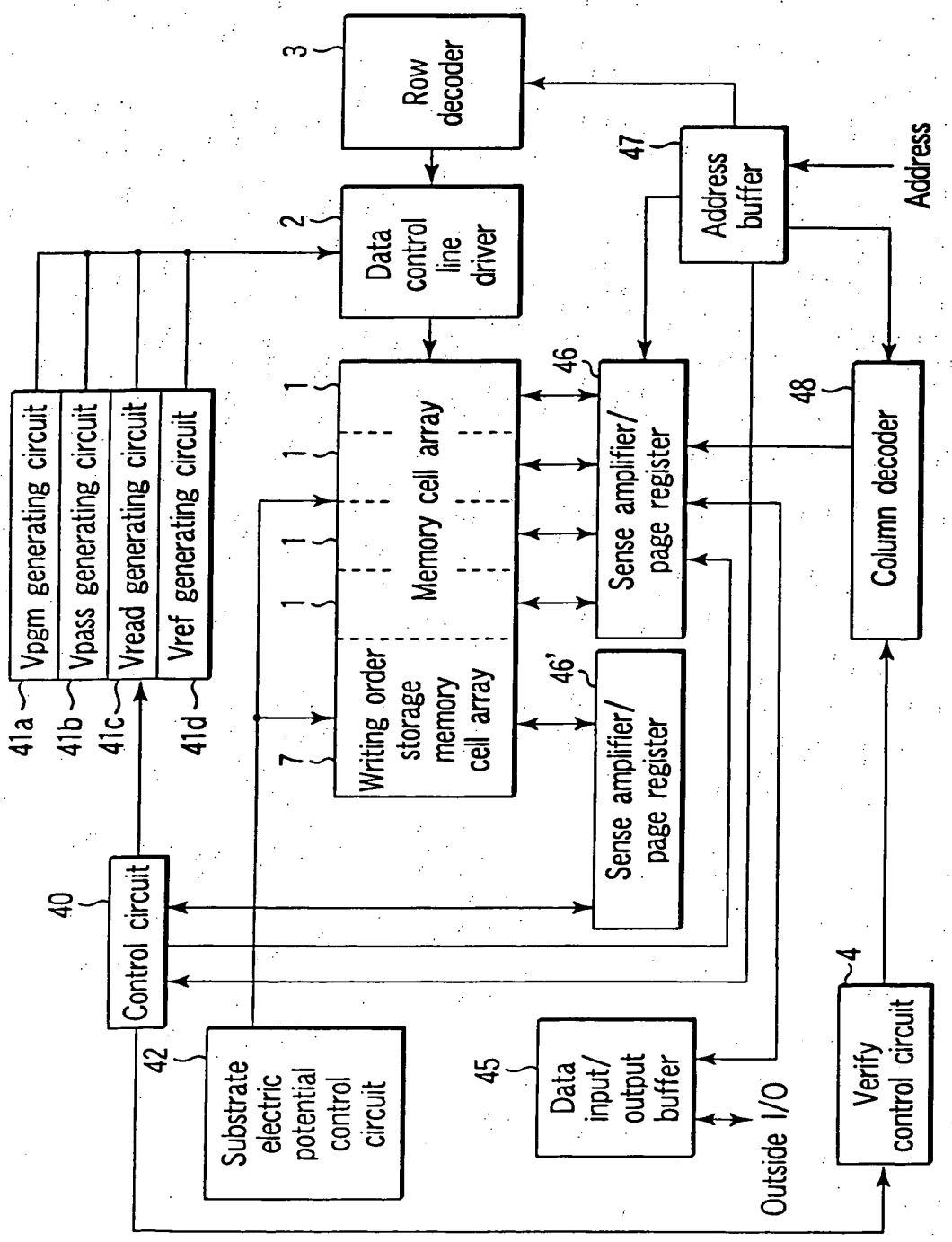
Row decoder
3
Data control line driver
2
Address buffer
47
Address
Memory cell array
1
Writing order storage memory cell array
7
Sense amplifier/ page register
46
Sense amplifier/ page register
46'
Column decoder
48
Vpgm generating circuit
Vpass generating circuit
Vread generating circuit
Vref generating circuit
41a
41b
41c
41d
Control circuit
40
Substrate electric potential control circuit
42
Data input/ output buffer
45
Outside I/O
Verify control circuit
4

FIG. 10

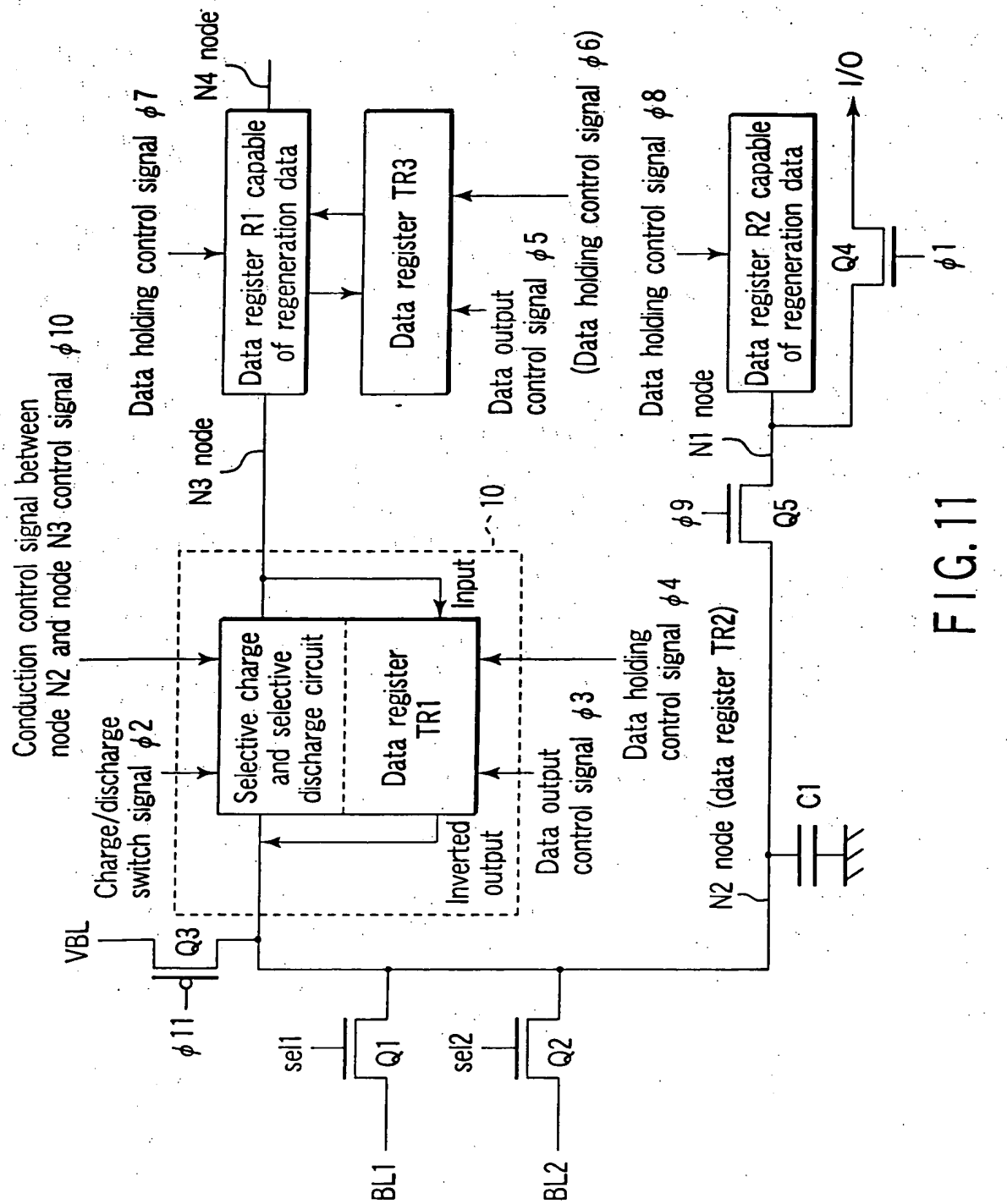
Conduction control signal between node N2 and node N3 control signal φ10
Charge/discharge switch signal φ2
VBL
Q3
φ11
sel1
Q1
BL1
sel2
Q2
BL2
Selective charge and selective discharge circuit
Data register TR1
Input
Inverted output
10
N3 node
Data holding control signal φ7
N4 node
Data register R1 capable of regeneration data
Data register TR3
Data output control signal φ5
(Data holding control signal φ6)
Data output control signal φ3
Data holding control signal φ4
N2 node (data register TR2)
C1
φ9
Q5
N1 node
Data holding control signal φ8
Data register R2 capable of regeneration data
Q4
φ1
I/O

FIG. 11

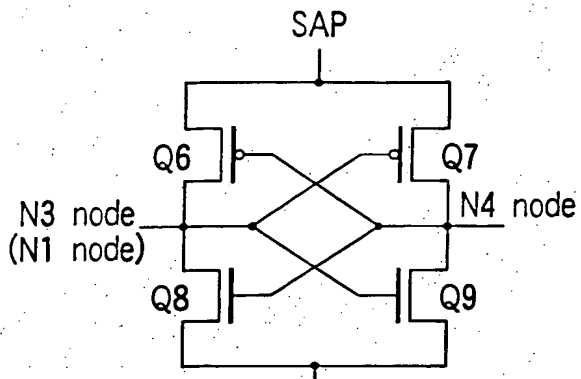

FIG. 12A

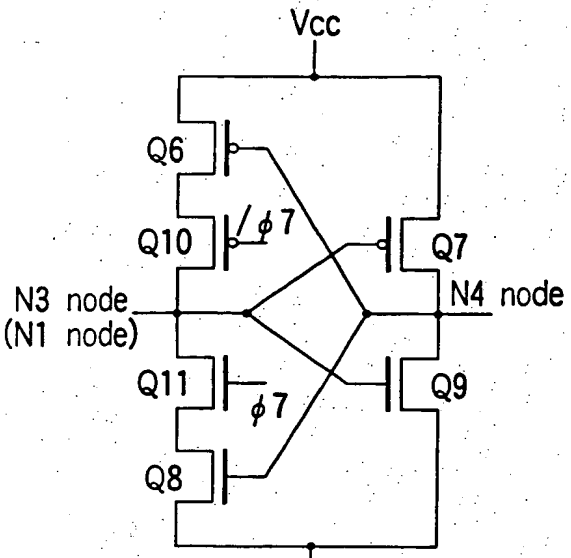

FIG. 12B

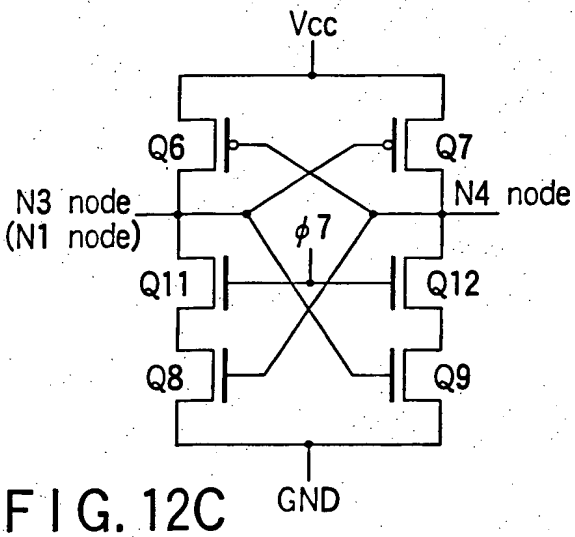

FIG. 12C

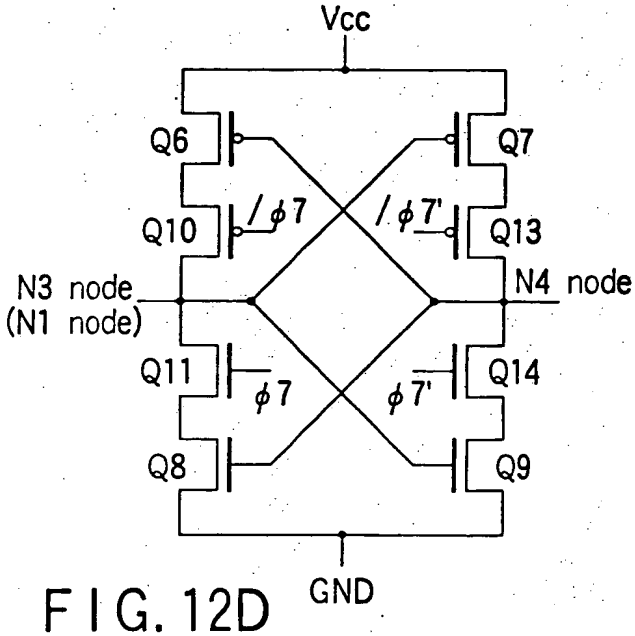

FIG. 12D

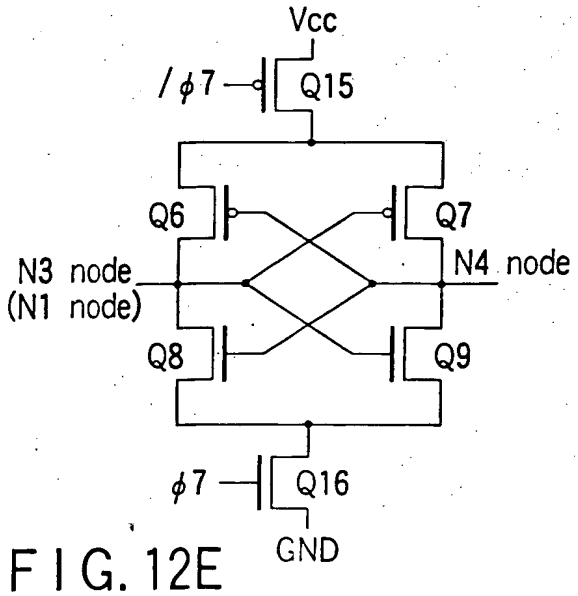

FIG. 12E

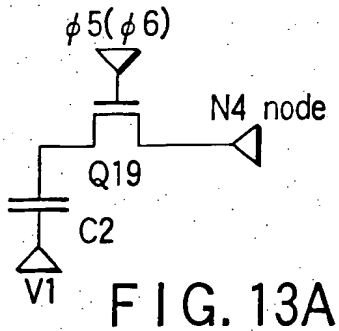

FIG. 13A

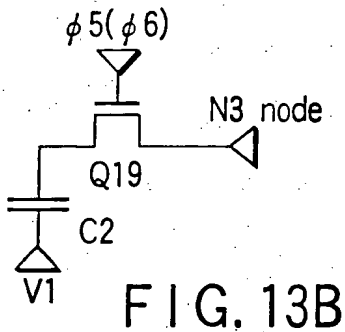

FIG. 13B

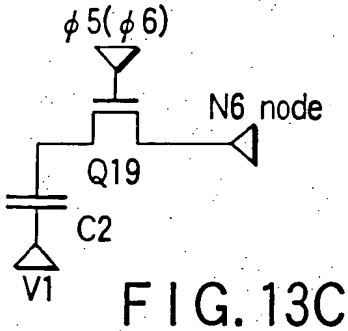

FIG. 13C

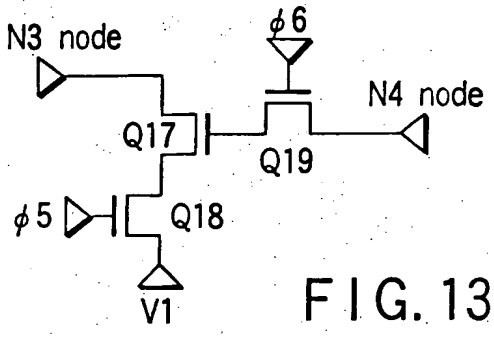

FIG. 13D

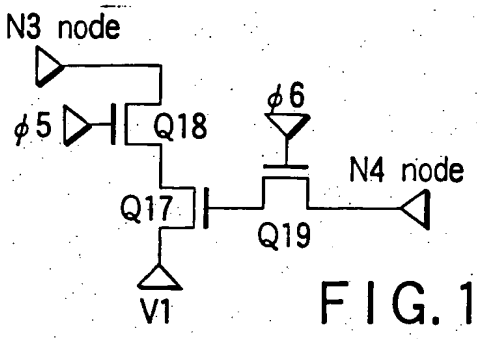

FIG. 13E

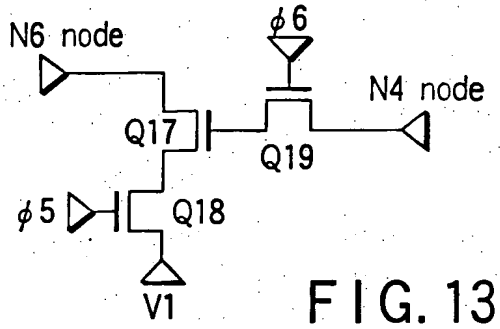

FIG. 13F

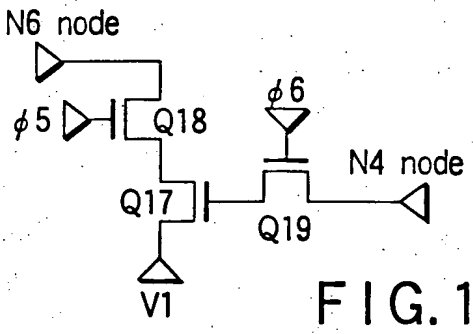

FIG. 13G

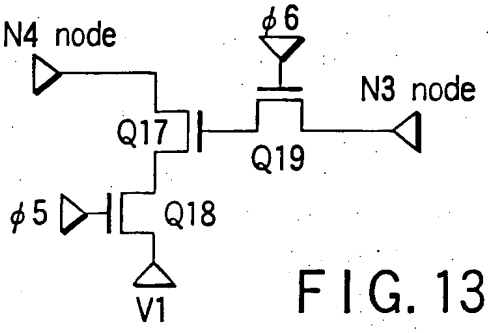

FIG. 13H

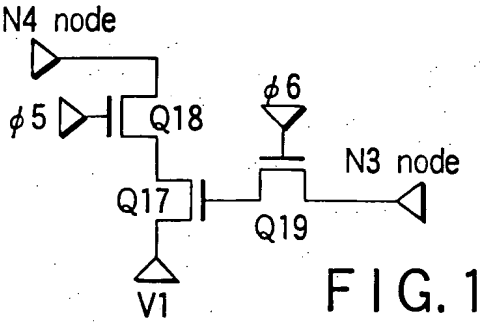

FIG. 13I

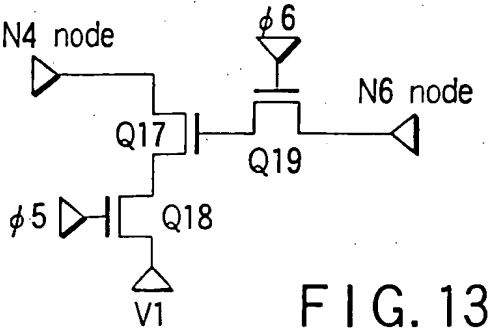

FIG. 13J

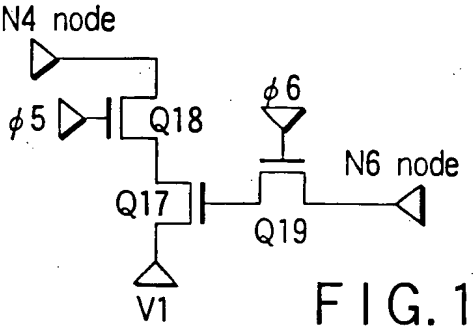

FIG. 13K

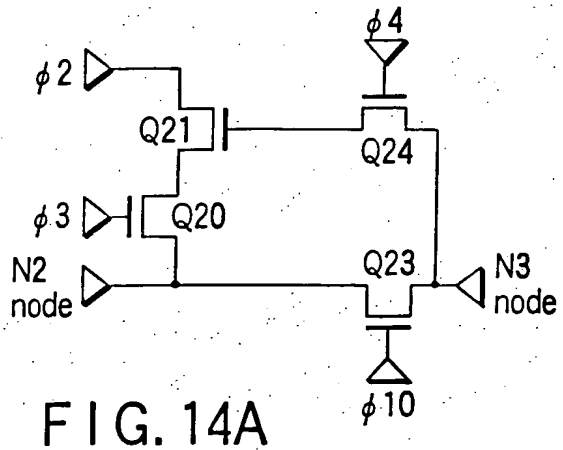

FIG. 14A

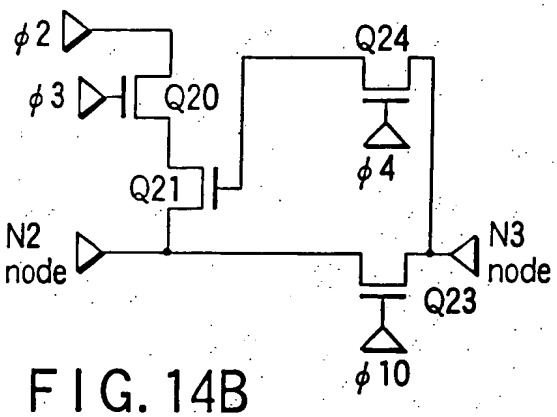

FIG. 14B

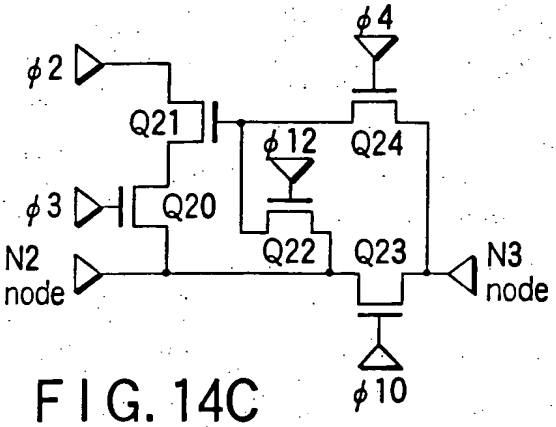

FIG. 14C

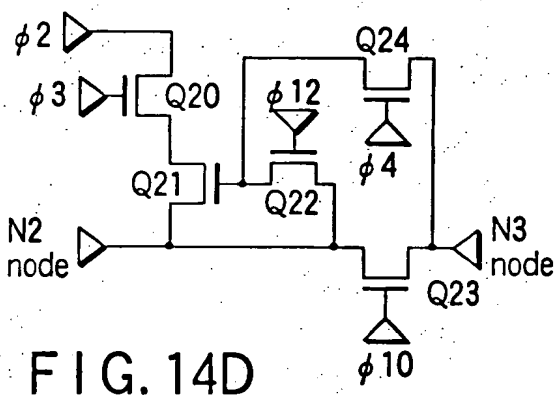

FIG. 14D

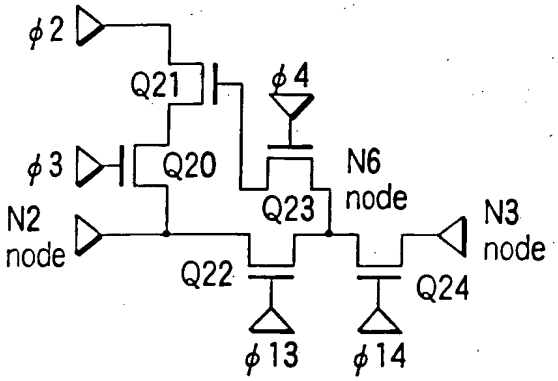

FIG. 14E

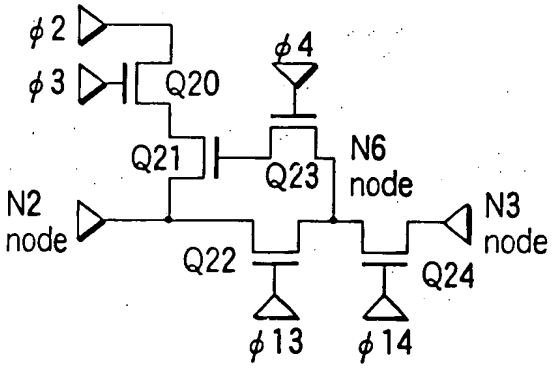

FIG. 14F

Q21 gate initial value (corresponding to TR1)	N2 node initial value	N2 node output after $\phi 3$="H"
"L"	"L"	"L"
"H"	"L"	"L"
"L"	"H"	"H"
"H"	"H"	"L"

In the case of $\phi 2$="L"
(selective discharge operation and inverted output operation)

FIG. 15A

Q21 gate initial value (corresponding to TR1)	N2 node initial value	N2 node output after $\phi 3$="H"
"L"	"L"	"L"
"H"	"L"	"H"
"L"	"H"	"H"
"H"	"H"	"H"

In the case of $\phi 2$="H"
(selective charge operation)

FIG. 15B

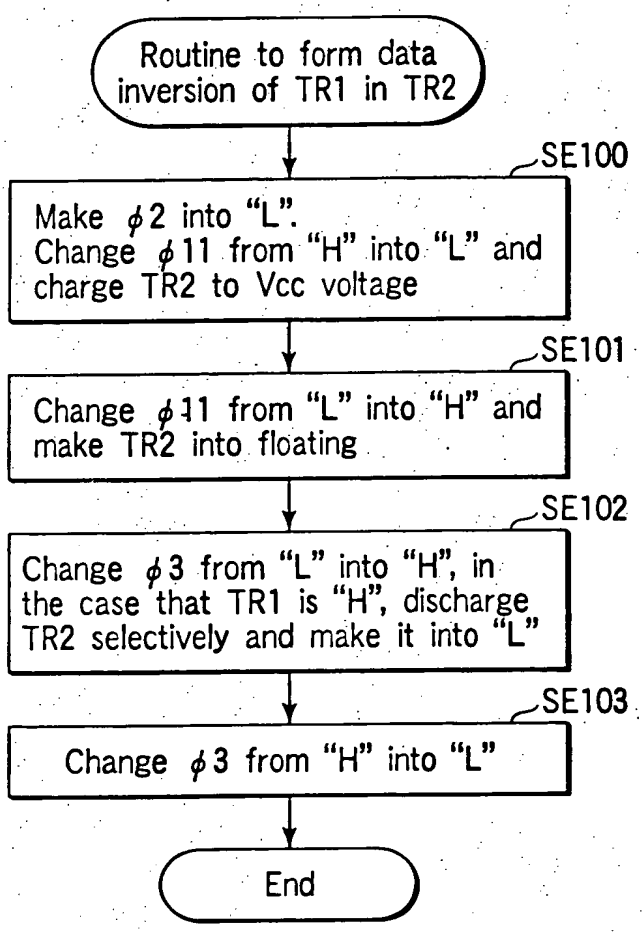
Routine to form data inversion of TR1 in TR2
SE100
Make φ2 into "L". Change φ11 from "H" into "L" and charge TR2 to Vcc voltage
SE101
Change φ11 from "L" into "H" and make TR2 into floating
SE102
Change φ3 from "L" into "H", in the case that TR1 is "H", discharge TR2 selectively and make it into "L"
SE103
Change φ3 from "H" into "L"
End

FIG. 16

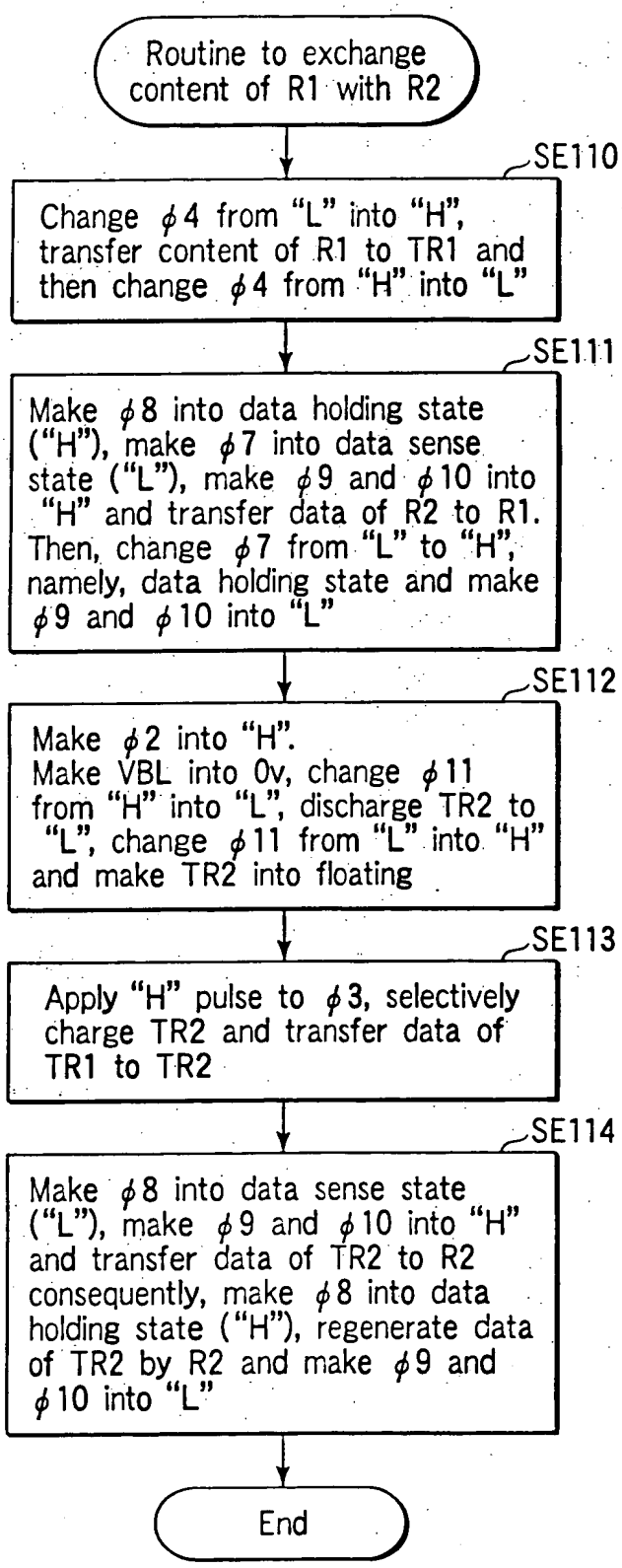
Routine to exchange content of R1 with R2
SE110
Change φ4 from "L" into "H", transfer content of R1 to TR1 and then change φ4 from "H" into "L"
SE111
Make φ8 into data holding state ("H"), make φ7 into data sense state ("L"), make φ9 and φ10 into "H" and transfer data of R2 to R1. Then, change φ7 from "L" to "H", namely, data holding state and make φ9 and φ10 into "L"
SE112
Make φ2 into "H". Make VBL into 0v, change φ11 from "H" into "L", discharge TR2 to "L", change φ11 from "L" into "H" and make TR2 into floating
SE113
Apply "H" pulse to φ3, selectively charge TR2 and transfer data of TR1 to TR2
SE114
Make φ8 into data sense state ("L"), make φ9 and φ10 into "H" and transfer data of TR2 to R2 consequently, make φ8 into data holding state ("H"), regenerate data of TR2 by R2 and make φ9 and φ10 into "L"
End

FIG. 17

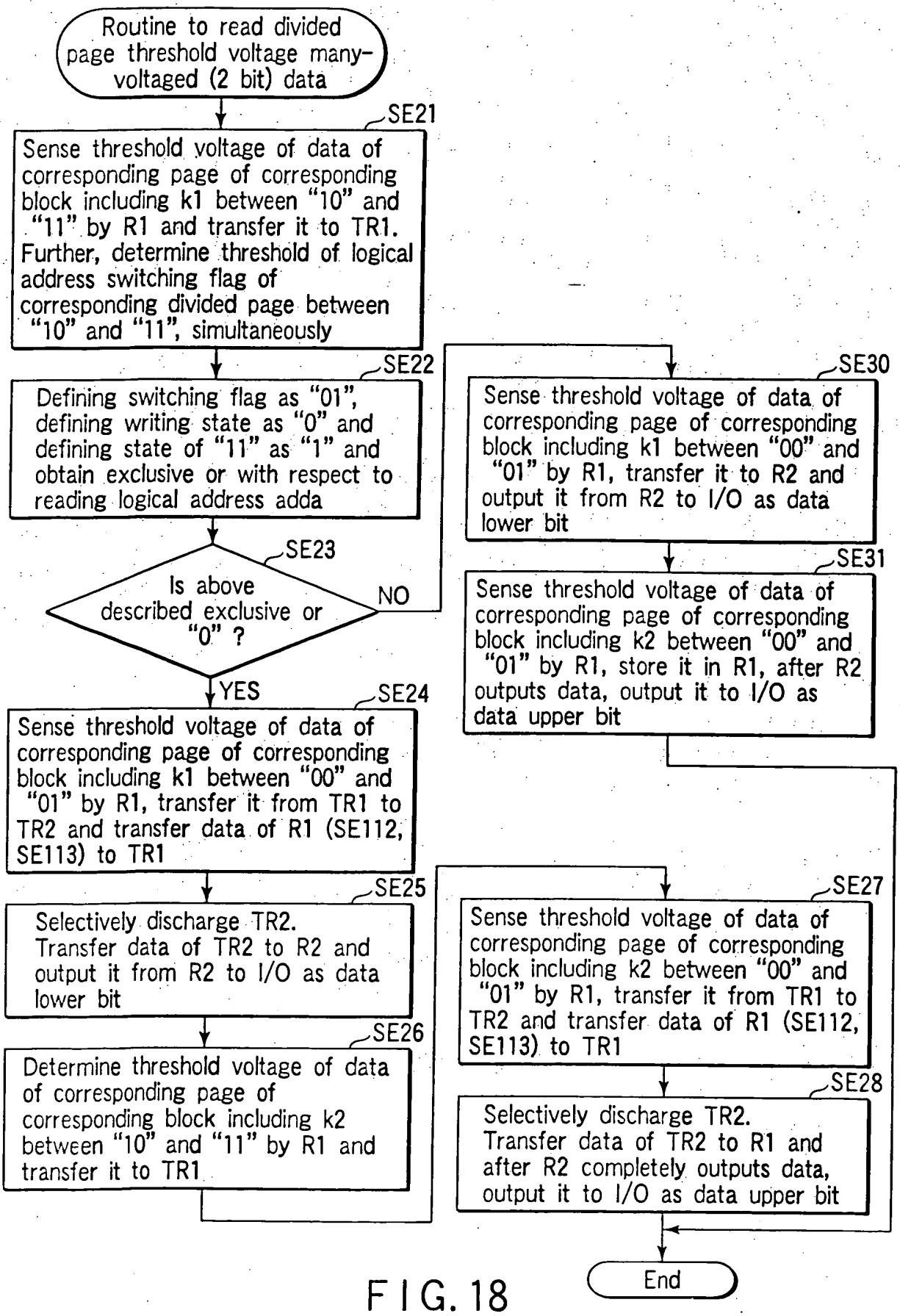
Routine to read divided page threshold voltage many-voltaged (2 bit) data
SE21
Sense threshold voltage of data of corresponding page of corresponding block including k1 between "10" and "11" by R1 and transfer it to TR1. Further, determine threshold of logical address switching flag of corresponding divided page between "10" and "11", simultaneously
SE22
Defining switching flag as "01", defining writing state as "0" and defining state of "11" as "1" and obtain exclusive or with respect to reading logical address adda
SE23
Is above described exclusive or "0" ?
NO
YES
SE24
Sense threshold voltage of data of corresponding page of corresponding block including k1 between "00" and "01" by R1, transfer it from TR1 to TR2 and transfer data of R1 (SE112, SE113) to TR1
SE25
Selectively discharge TR2. Transfer data of TR2 to R2 and output it from R2 to I/O as data lower bit
SE26
Determine threshold voltage of data of corresponding page of corresponding block including k2 between "10" and "11" by R1 and transfer it to TR1
SE30
Sense threshold voltage of data of corresponding page of corresponding block including k1 between "00" and "01" by R1, transfer it to R2 and output it from R2 to I/O as data lower bit
SE31
Sense threshold voltage of data of corresponding page of corresponding block including k2 between "00" and "01" by R1, store it in R1, after R2 outputs data, output it to I/O as data upper bit
SE27
Sense threshold voltage of data of corresponding page of corresponding block including k2 between "00" and "01" by R1, transfer it from TR1 to TR2 and transfer data of R1 (SE112, SE113) to TR1
SE28
Selectively discharge TR2. Transfer data of TR2 to R1 and after R2 completely outputs data, output it to I/O as data upper bit
End

FIG. 18

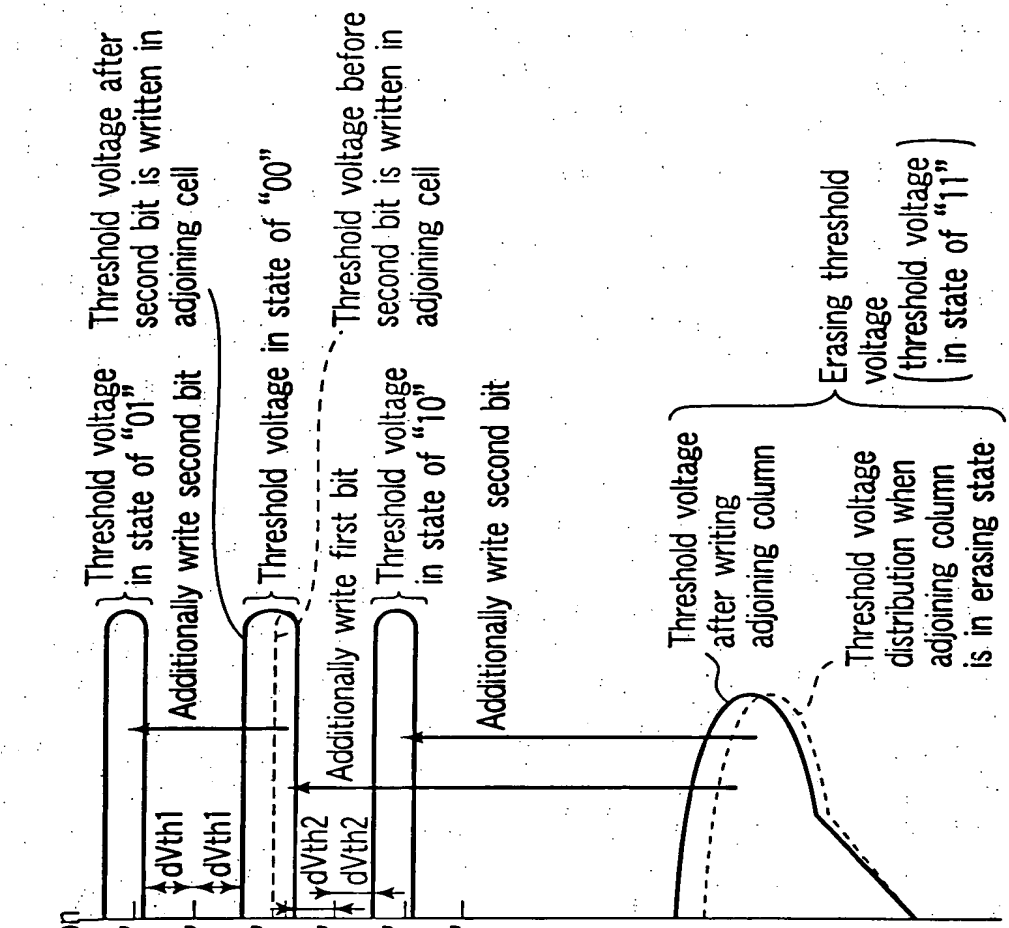
Memory cell transistor threshold voltage distribution
Verify reference threshold voltage in states of "01" and "00"
Reading reference threshold voltage in states of "01" and "00"
Verify reference threshold voltage in states of "00" and "10"
Reading reference threshold voltage in states of "00" and "10"
Verify reference threshold voltage in states of "10" and "11"
Reading reference threshold voltage in states of "10" and "11"
dVth1
dVth1
dVth2
dVth2
Threshold voltage in state of "01"
Additionally write second bit
Threshold voltage after second bit is written in adjoining cell
Threshold voltage in state of "00"
Additionally write first bit
Threshold voltage before second bit is written in adjoining cell
Threshold voltage in state of "10"
Additionally write second bit
Threshold voltage after writing adjoining column
Threshold voltage distribution when adjoining column is in erasing state
Erasing threshold voltage (threshold voltage in state of "11")

FIG. 19

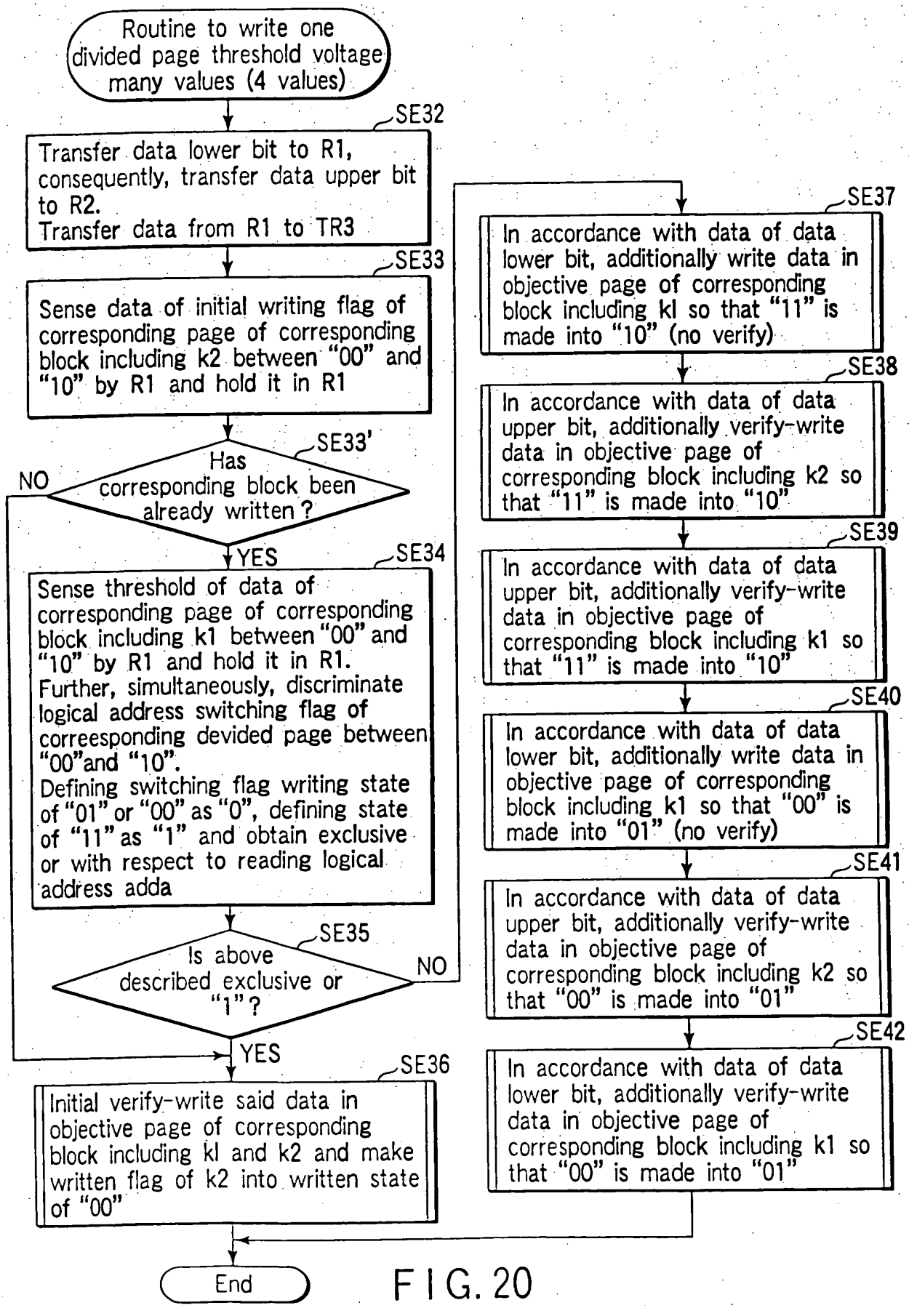
Routine to write one divided page threshold voltage many values (4 values)
SE32
Transfer data lower bit to R1, consequently, transfer data upper bit to R2.
Transfer data from R1 to TR3
SE33
Sense data of initial writing flag of corresponding page of corresponding block including k2 between "00" and "10" by R1 and hold it in R1
SE33'
Has corresponding block been already written ?
NO
YES
SE34
Sense threshold of data of corresponding page of corresponding block including k1 between "00" and "10" by R1 and hold it in R1.
Further, simultaneously, discriminate logical address switching flag of correesponding devided page between "00"and "10".
Defining switching flag writing state of "01" or "00" as "0", defining state of "11" as "1" and obtain exclusive or with respect to reading logical address adda
SE35
Is above described exclusive or "1"?
NO
YES
SE36
Initial verify-write said data in objective page of corresponding block including kl and k2 and make written flag of k2 into written state of "00"
SE37
In accordance with data of data lower bit, additionally write data in objective page of corresponding block including kl so that "11" is made into "10" (no verify)
SE38
In accordance with data of data upper bit, additionally verify-write data in objective page of corresponding block including k2 so that "11" is made into "10"
SE39
In accordance with data of data upper bit, additionally verify-write data in objective page of corresponding block including k1 so that "11" is made into "10"
SE40
In accordance with data of data lower bit, additionally write data in objective page of corresponding block including k1 so that "00" is made into "01" (no verify)
SE41
In accordance with data of data upper bit, additionally verify-write data in objective page of corresponding block including k2 so that "00" is made into "01"
SE42
In accordance with data of data lower bit, additionally verify-write data in objective page of corresponding block including k1 so that "00" is made into "01"
End

FIG. 20

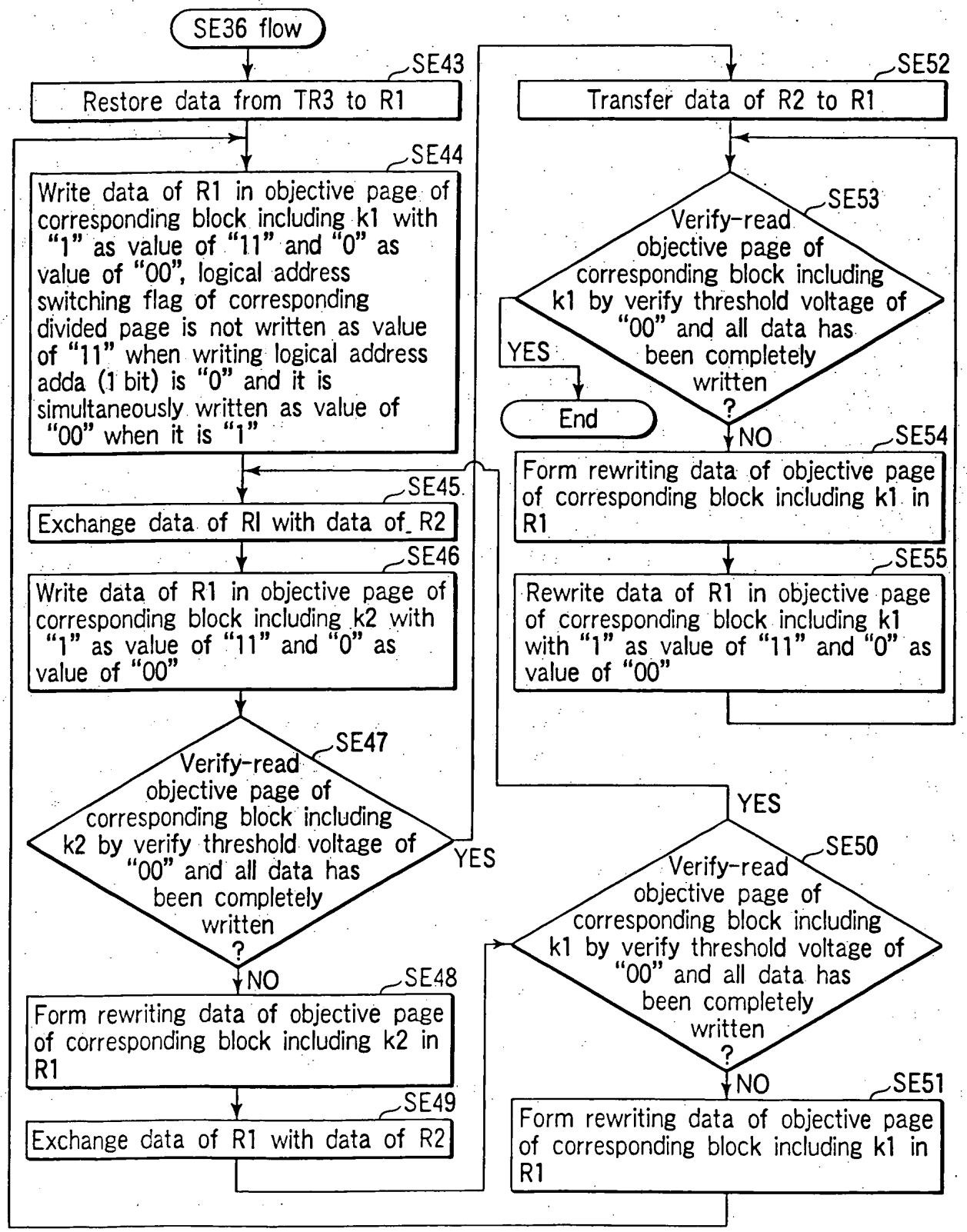
SE36 flow
SE43
Restore data from TR3 to R1
SE44
Write data of R1 in objective page of corresponding block including k1 with "1" as value of "11" and "0" as value of "00", logical address switching flag of corresponding divided page is not written as value of "11" when writing logical address adda (1 bit) is "0" and it is simultaneously written as value of "00" when it is "1"
SE45
Exchange data of RI with data of R2
SE46
Write data of R1 in objective page of corresponding block including k2 with "1" as value of "11" and "0" as value of "00"
SE47
Verify-read objective page of corresponding block including k2 by verify threshold voltage of "00" and all data has been completely written ?
YES
NO
SE48
Form rewriting data of objective page of corresponding block including k2 in R1
SE49
Exchange data of R1 with data of R2
SE52
Transfer data of R2 to R1
SE53
Verify-read objective page of corresponding block including k1 by verify threshold voltage of "00" and all data has been completely written ?
YES
End
NO
SE54
Form rewriting data of objective page of corresponding block including k1 in R1
SE55
Rewrite data of R1 in objective page of corresponding block including k1 with "1" as value of "11" and "0" as value of "00"
YES
SE50
Verify-read objective page of corresponding block including k1 by verify threshold voltage of "00" and all data has been completely written ?
NO
SE51
Form rewriting data of objective page of corresponding block including k1 in R1

FIG. 21

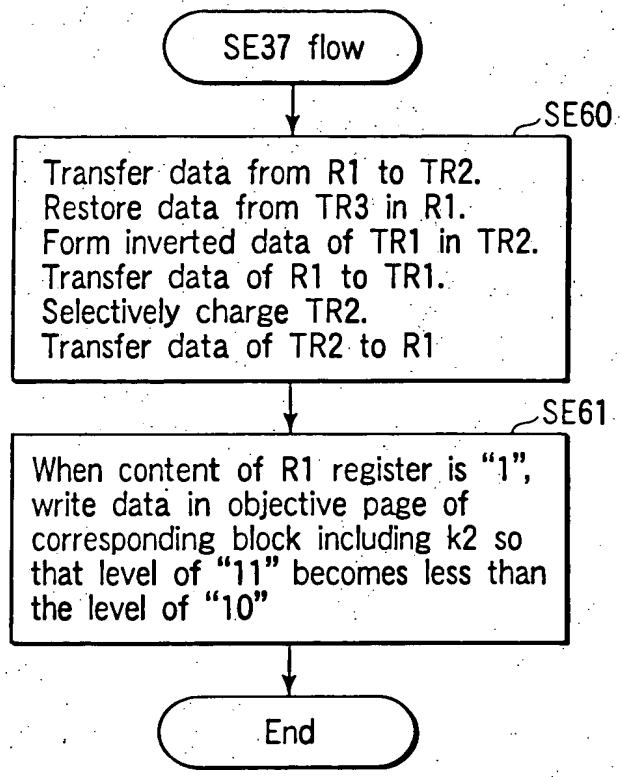
SE37 flow
SE60
Transfer data from R1 to TR2.
Restore data from TR3 in R1.
Form inverted data of TR1 in TR2.
Transfer data of R1 to TR1.
Selectively charge TR2.
Transfer data of TR2 to R1
SE61
When content of R1 register is "1", write data in objective page of corresponding block including k2 so that level of "11" becomes less than the level of "10"
End

FIG. 22

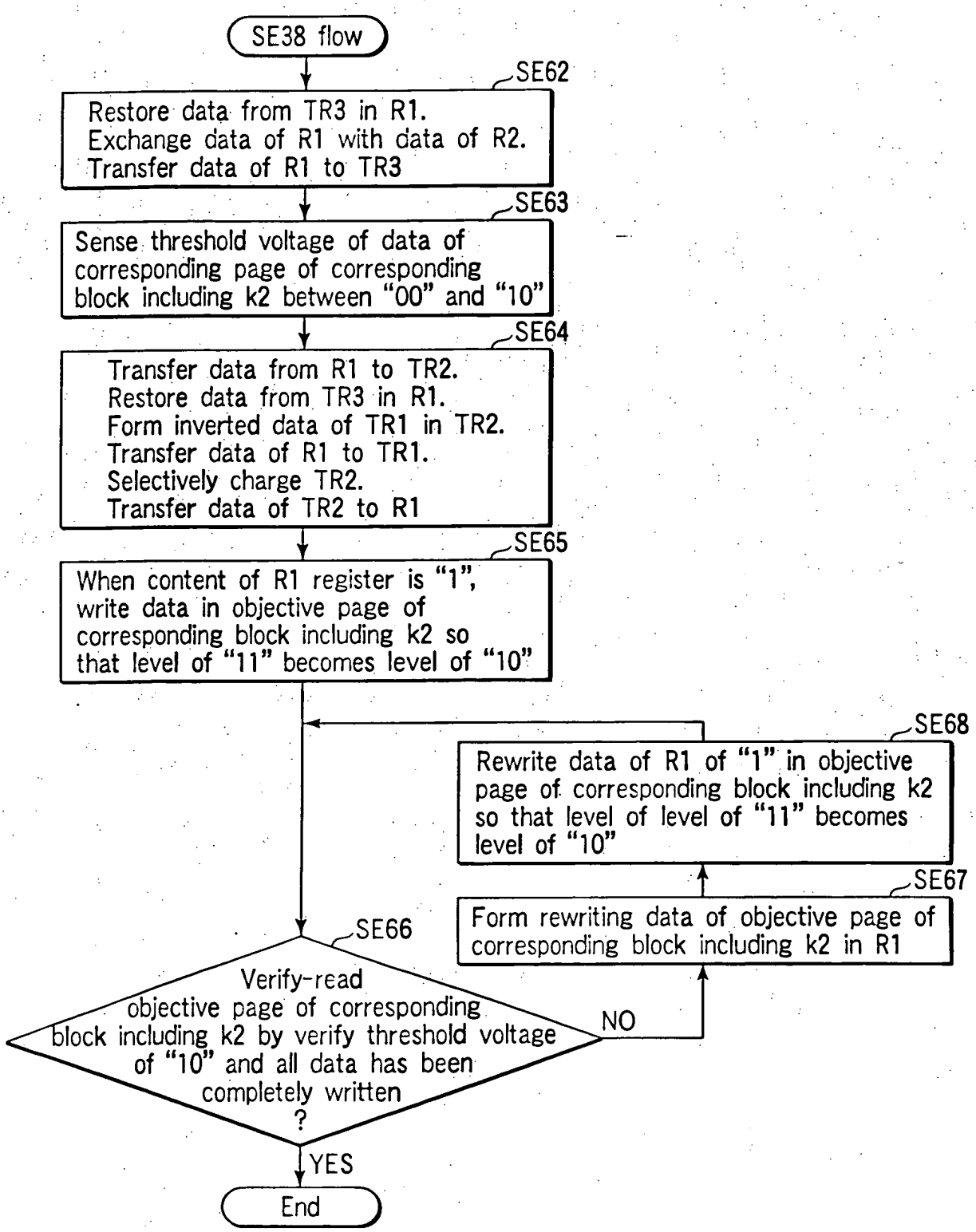
SE38 flow
SE62
Restore data from TR3 in R1.
Exchange data of R1 with data of R2.
Transfer data of R1 to TR3
SE63
Sense threshold voltage of data of corresponding page of corresponding block including k2 between "00" and "10"
SE64
Transfer data from R1 to TR2.
Restore data from TR3 in R1.
Form inverted data of TR1 in TR2.
Transfer data of R1 to TR1.
Selectively charge TR2.
Transfer data of TR2 to R1
SE65
When content of R1 register is "1", write data in objective page of corresponding block including k2 so that level of "11" becomes level of "10"
SE68
Rewrite data of R1 of "1" in objective page of corresponding block including k2 so that level of level of "11" becomes level of "10"
SE67
Form rewriting data of objective page of corresponding block including k2 in R1
SE66
Verify-read objective page of corresponding block including k2 by verify threshold voltage of "10" and all data has been completely written ?
NO
YES
End

FIG. 23

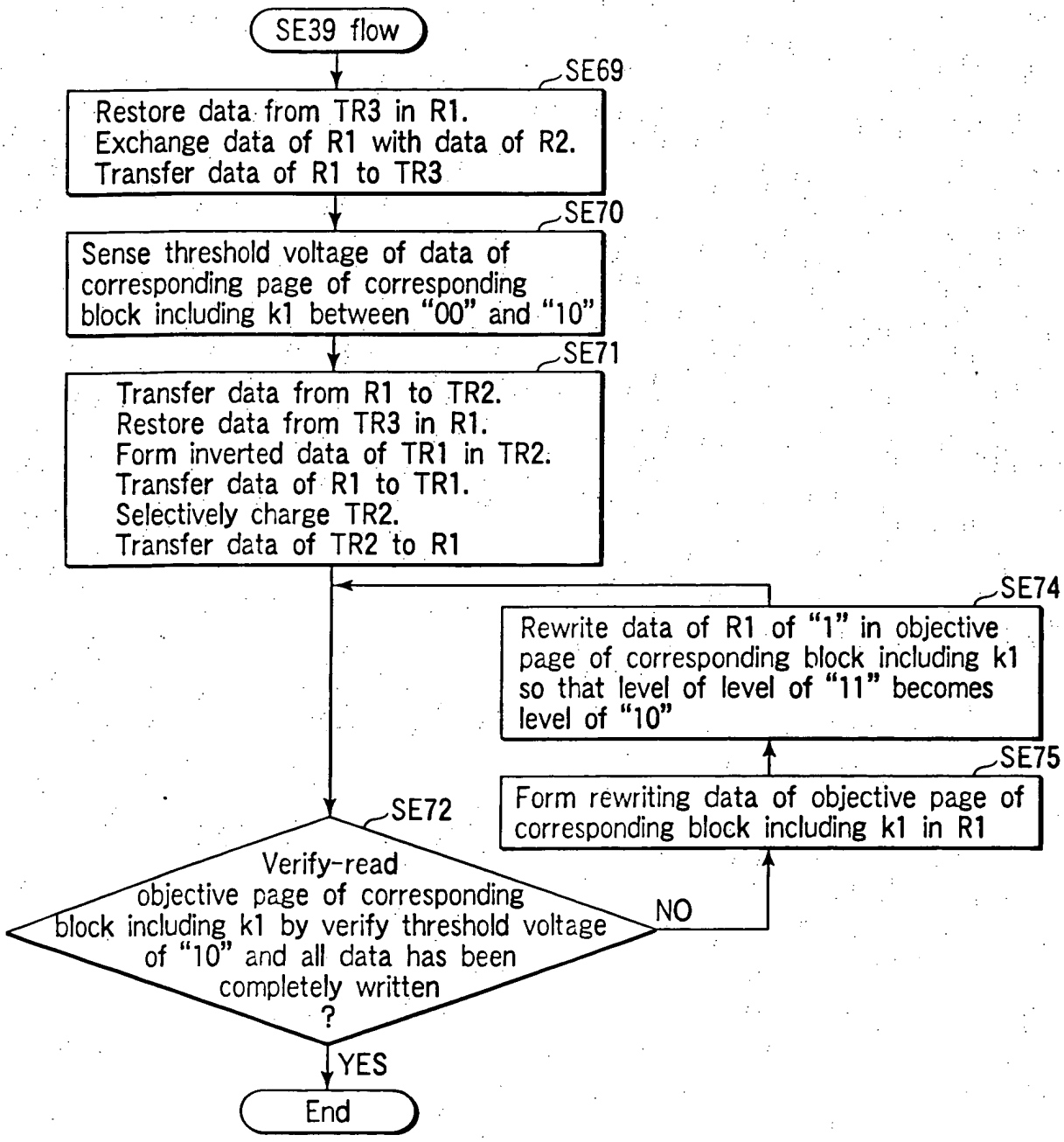
SE39 flow
SE69
Restore data from TR3 in R1.
Exchange data of R1 with data of R2.
Transfer data of R1 to TR3
SE70
Sense threshold voltage of data of corresponding page of corresponding block including k1 between "00" and "10"
SE71
Transfer data from R1 to TR2.
Restore data from TR3 in R1.
Form inverted data of TR1 in TR2.
Transfer data of R1 to TR1.
Selectively charge TR2.
Transfer data of TR2 to R1
SE74
Rewrite data of R1 of "1" in objective page of corresponding block including k1 so that level of level of "11" becomes level of "10"
SE75
Form rewriting data of objective page of corresponding block including k1 in R1
SE72
Verify-read objective page of corresponding block including k1 by verify threshold voltage of "10" and all data has been completely written ?
NO
YES
End

FIG. 24

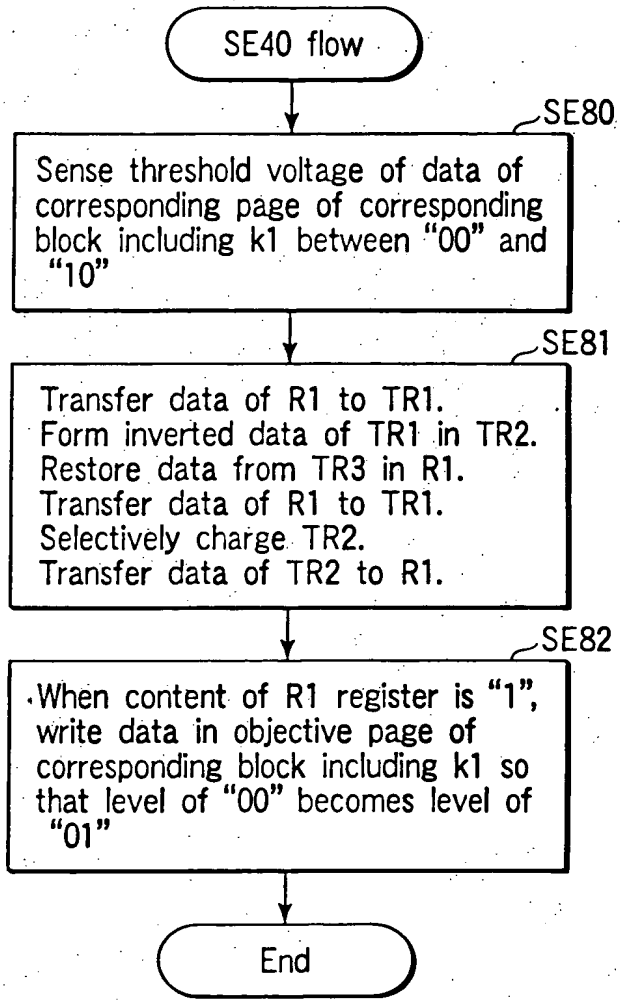
SE40 flow
SE80
Sense threshold voltage of data of corresponding page of corresponding block including k1 between "00" and "10"
SE81
Transfer data of R1 to TR1.
Form inverted data of TR1 in TR2.
Restore data from TR3 in R1.
Transfer data of R1 to TR1.
Selectively charge TR2.
Transfer data of TR2 to R1.
SE82
When content of R1 register is "1", write data in objective page of corresponding block including k1 so that level of "00" becomes level of "01"
End

FIG. 25

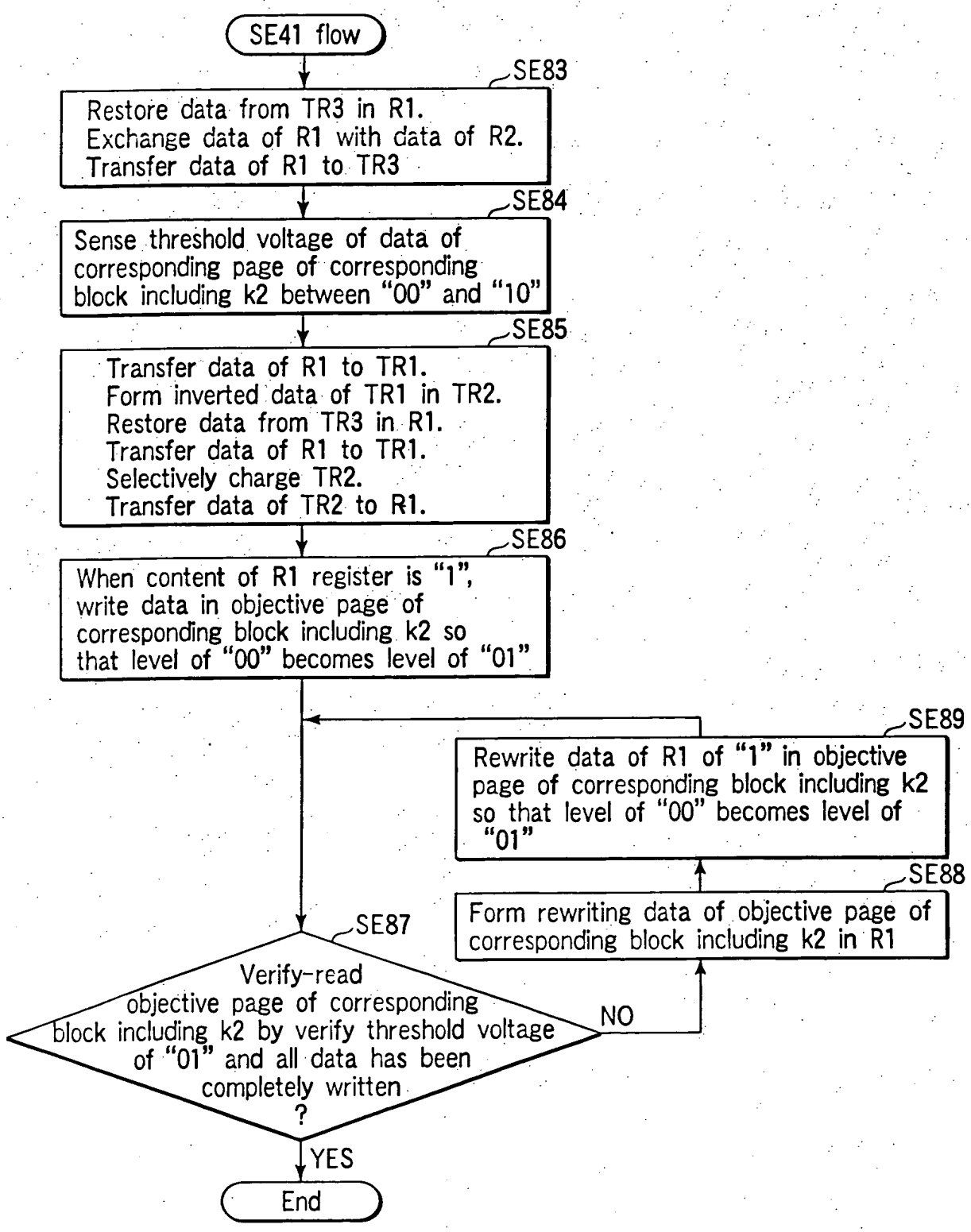
SE41 flow
SE83
Restore data from TR3 in R1.
Exchange data of R1 with data of R2.
Transfer data of R1 to TR3
SE84
Sense threshold voltage of data of corresponding page of corresponding block including k2 between "00" and "10"
SE85
Transfer data of R1 to TR1.
Form inverted data of TR1 in TR2.
Restore data from TR3 in R1.
Transfer data of R1 to TR1.
Selectively charge TR2.
Transfer data of TR2 to R1.
SE86
When content of R1 register is "1", write data in objective page of corresponding block including k2 so that level of "00" becomes level of "01"
SE89
Rewrite data of R1 of "1" in objective page of corresponding block including k2 so that level of "00" becomes level of "01"
SE88
Form rewriting data of objective page of corresponding block including k2 in R1
SE87
Verify-read objective page of corresponding block including k2 by verify threshold voltage of "01" and all data has been completely written ?
NO
YES
End

FIG. 26

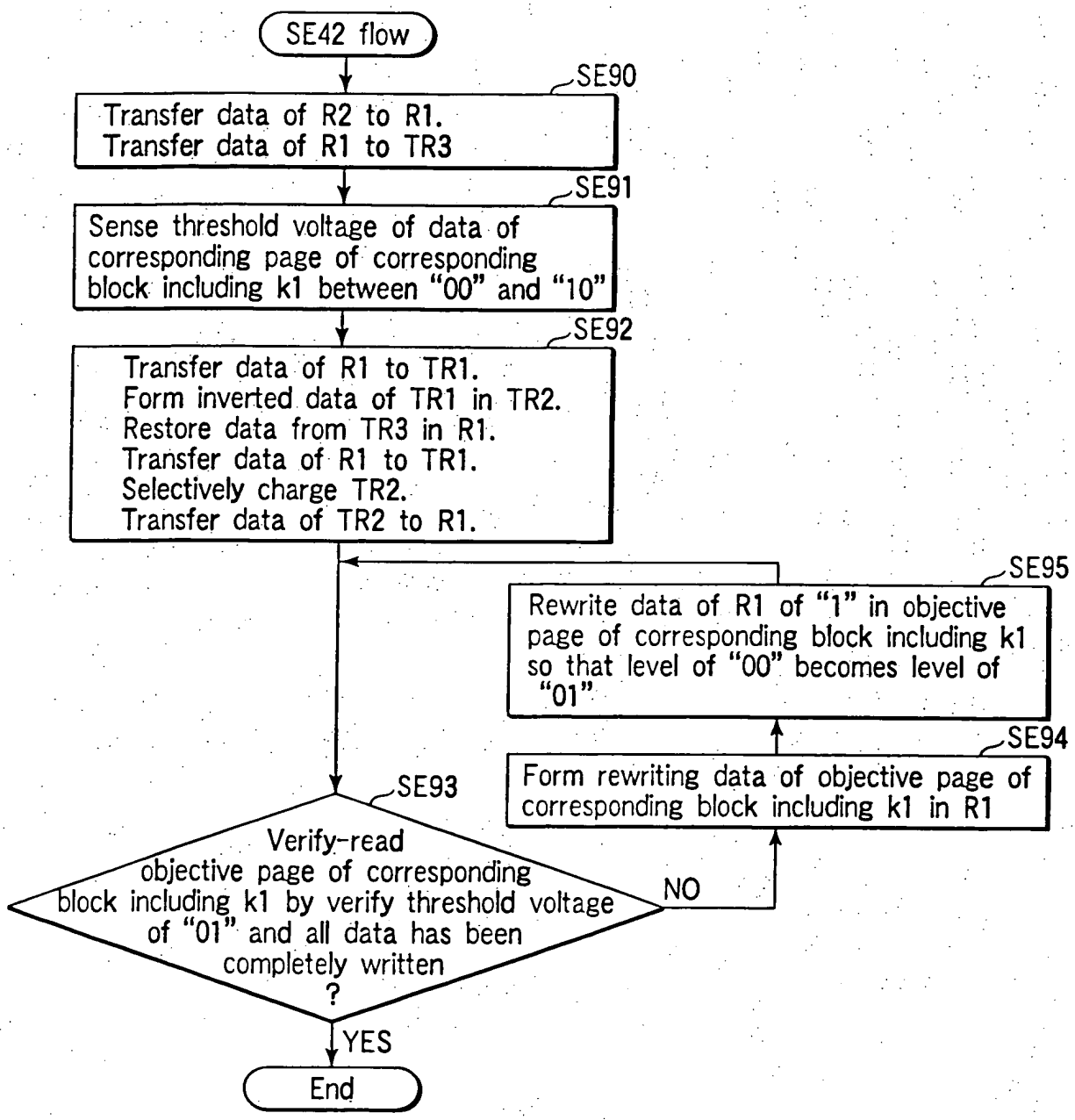
SE42 flow
SE90
Transfer data of R2 to R1.
Transfer data of R1 to TR3
SE91
Sense threshold voltage of data of corresponding page of corresponding block including k1 between "00" and "10"
SE92
Transfer data of R1 to TR1.
Form inverted data of TR1 in TR2.
Restore data from TR3 in R1.
Transfer data of R1 to TR1.
Selectively charge TR2.
Transfer data of TR2 to R1.
SE95
Rewrite data of R1 of "1" in objective page of corresponding block including k1 so that level of "00" becomes level of "01"
SE94
Form rewriting data of objective page of corresponding block including k1 in R1
SE93
Verify-read objective page of corresponding block including k1 by verify threshold voltage of "01" and all data has been completely written ?
NO
YES
End

FIG. 27

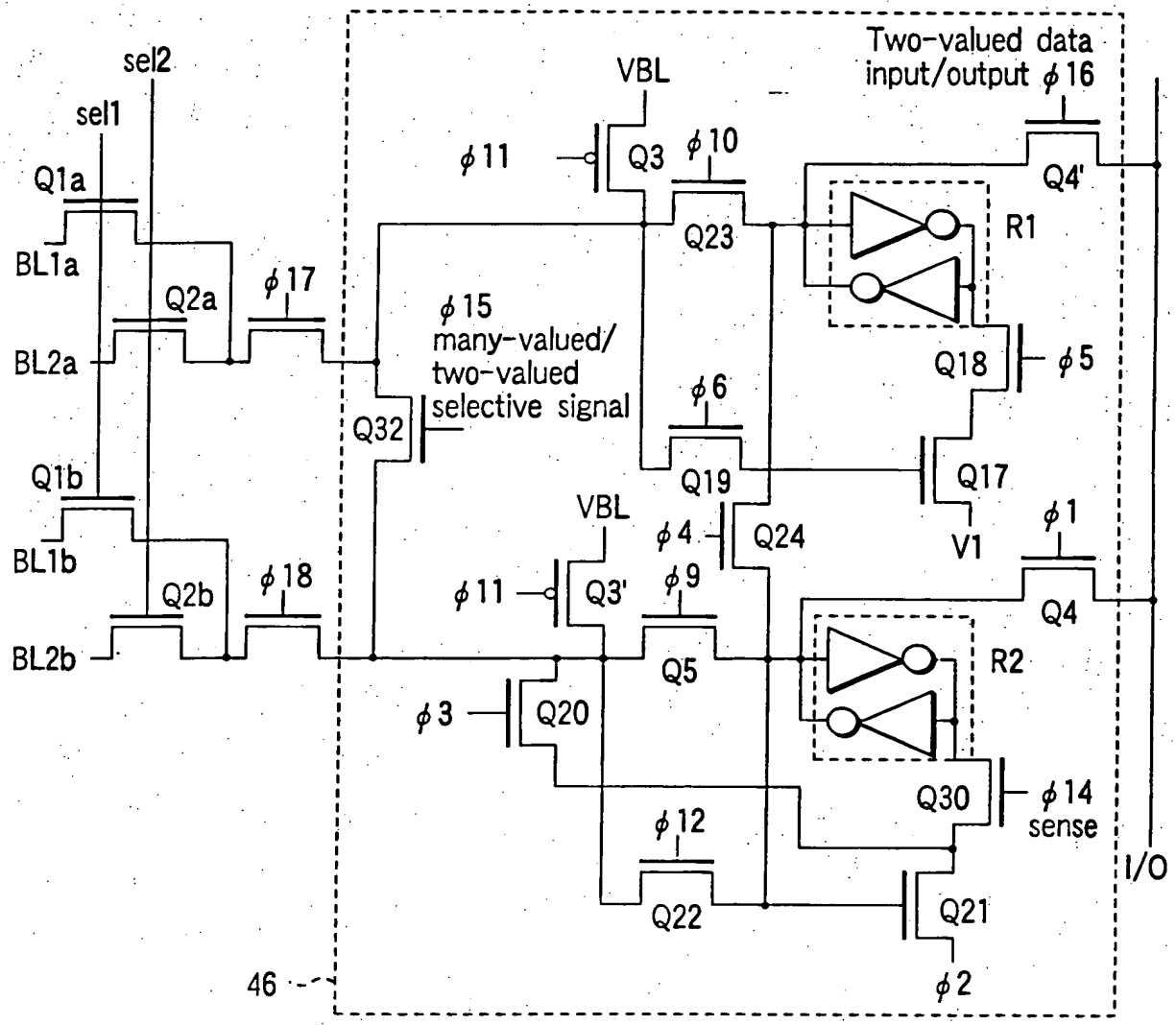
sel2
sel1
Q1a
BL1a
Q2a
BL2a
Q1b
BL1b
Q2b
BL2b
φ17
φ18
φ15
many-valued/
two-valued
selective signal
Q32
VBL
φ11
Q3
φ10
Q23
φ6
Q19
VBL
φ11
Q3'
φ9
Q5
φ3
Q20
φ4
Q24
φ12
Q22
Two-valued data
input/output φ16
Q4'
R1
Q18
φ5
Q17
V1
φ1
Q4
R2
Q30
φ14
sense
Q21
φ2
I/O
46

FIG. 28

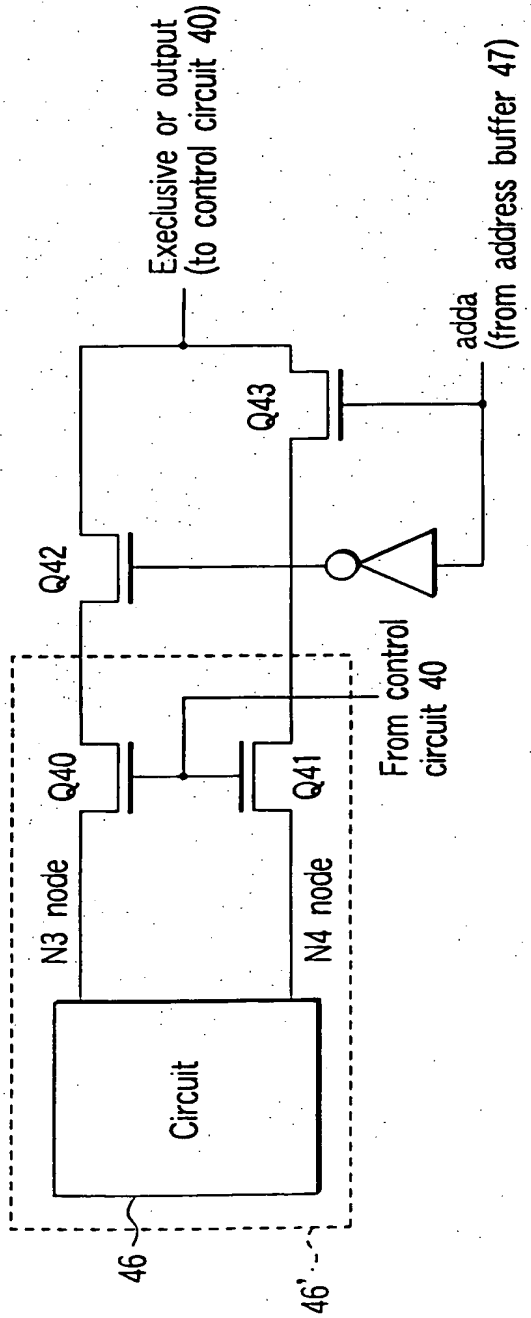
Exclusive or output
(to control circuit 40)
adda
(from address buffer 47)
Q43
Q42
From control
circuit 40
Q40
Q41
N3 node
N4 node
Circuit
46
46'

FIG. 29

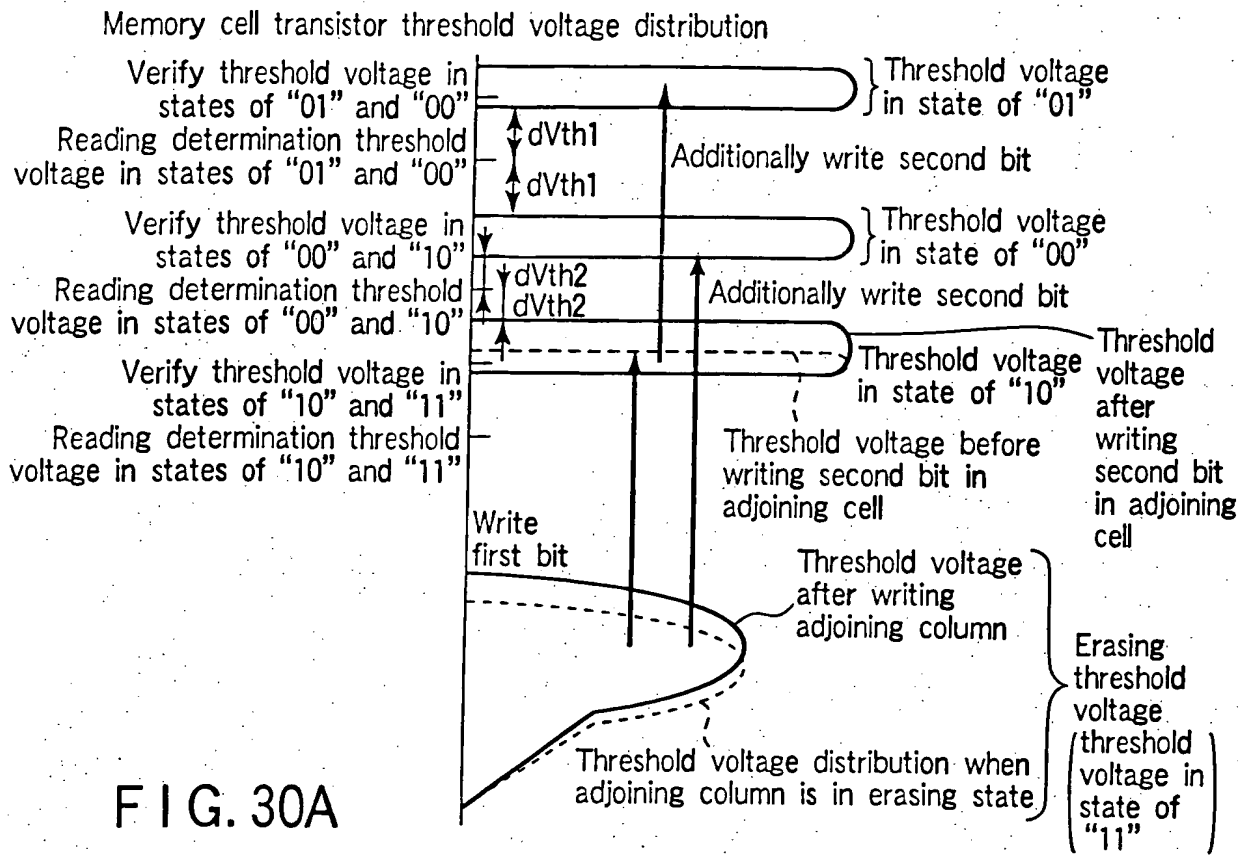

FIG. 30A

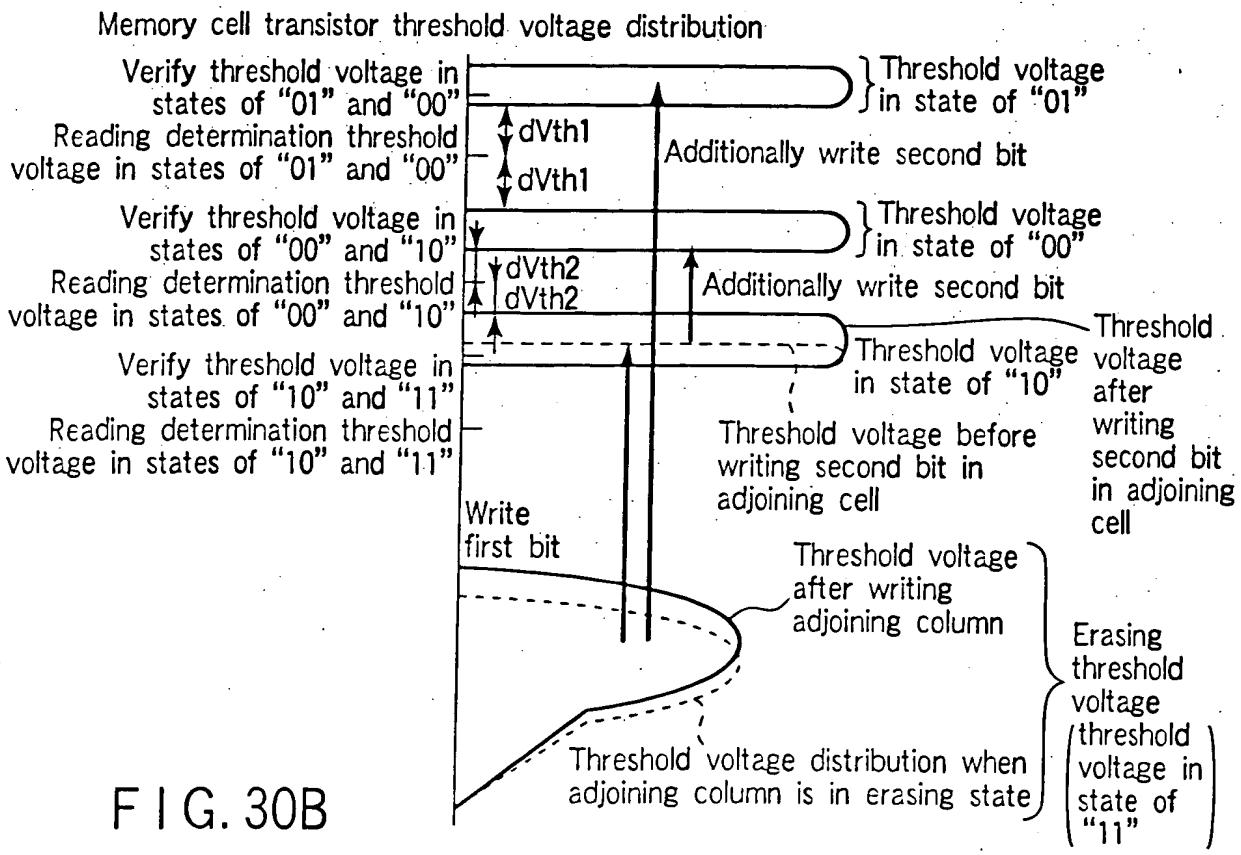

FIG. 30B

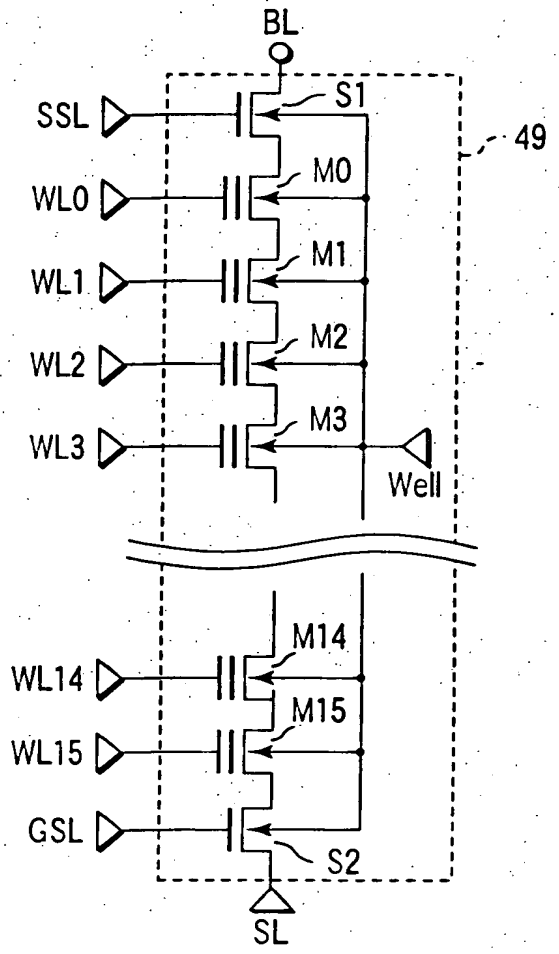

FIG. 31A

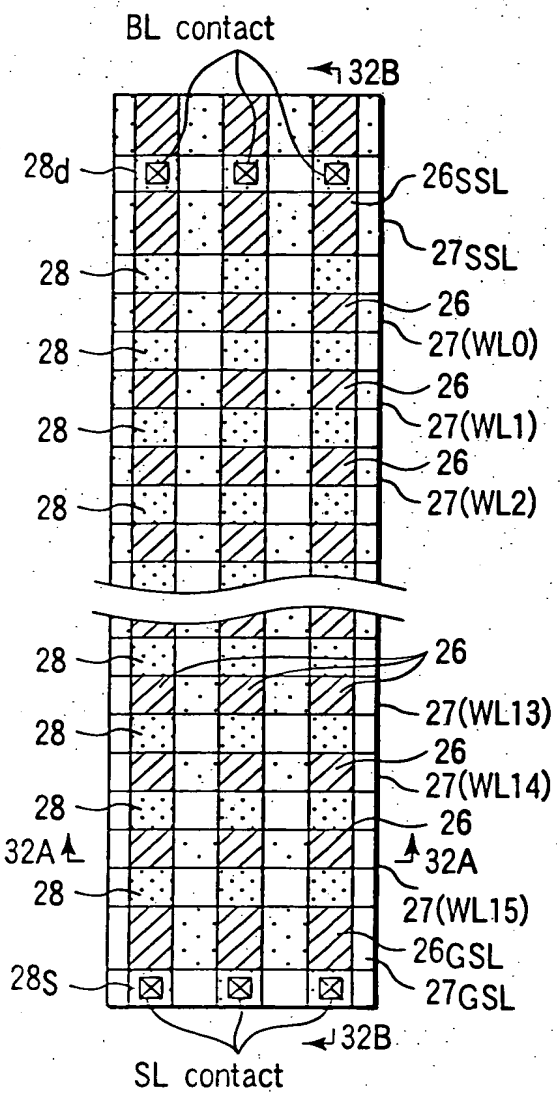

FIG. 31B

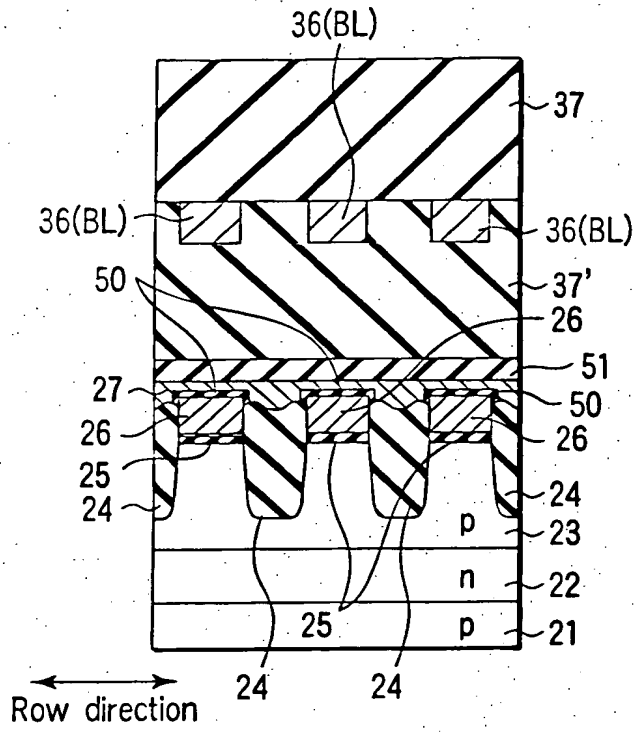

FIG. 32A

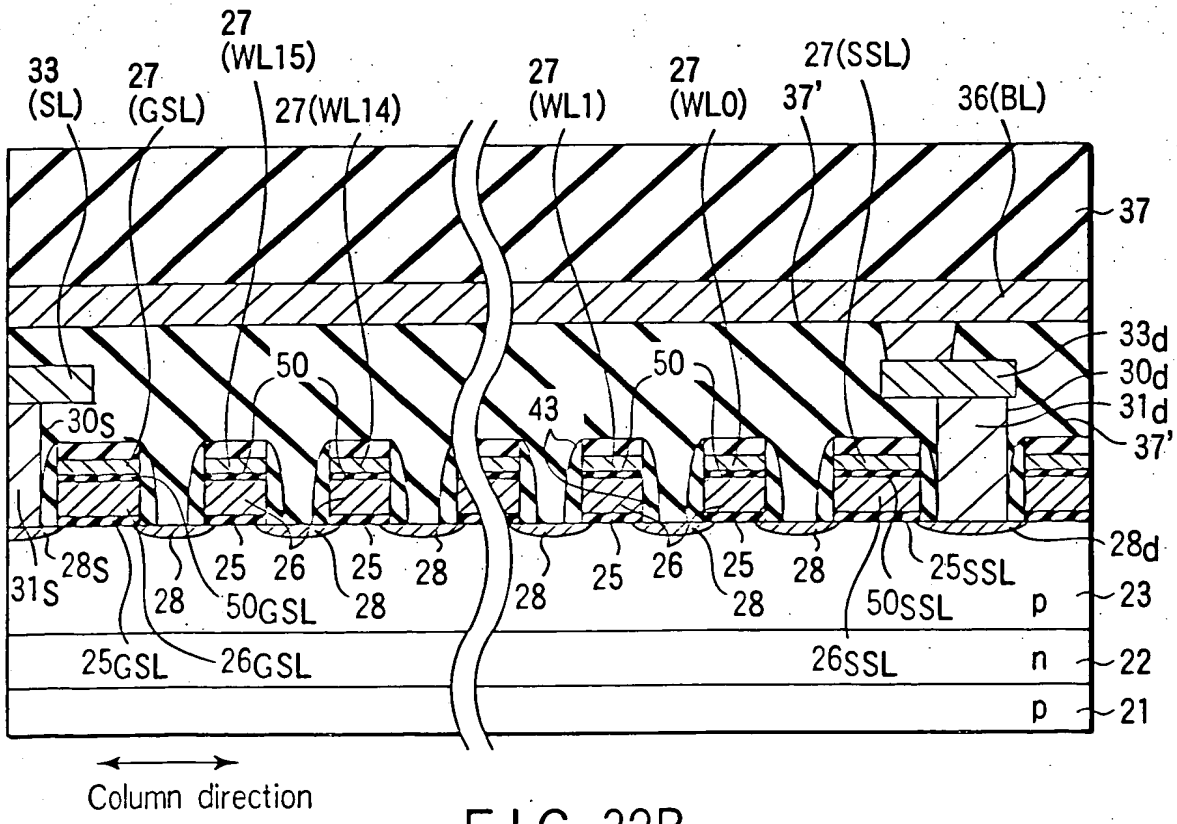

FIG. 32B

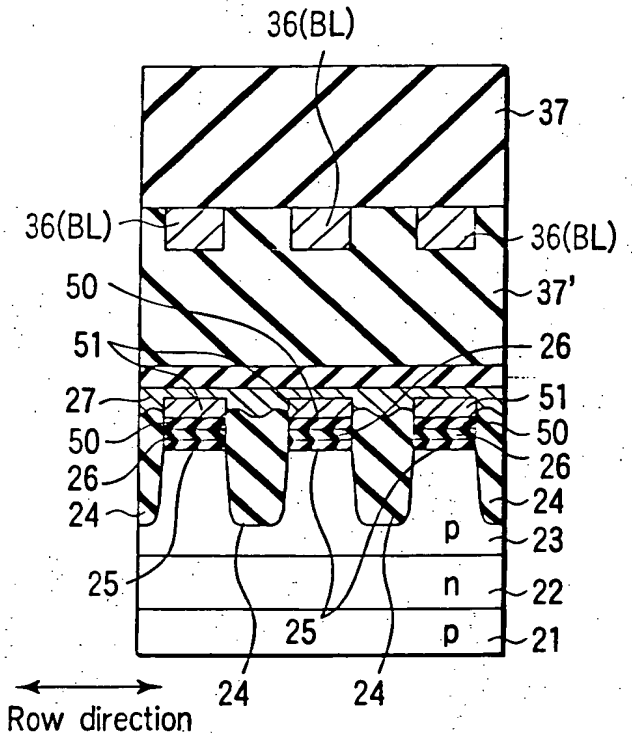

FIG. 33A

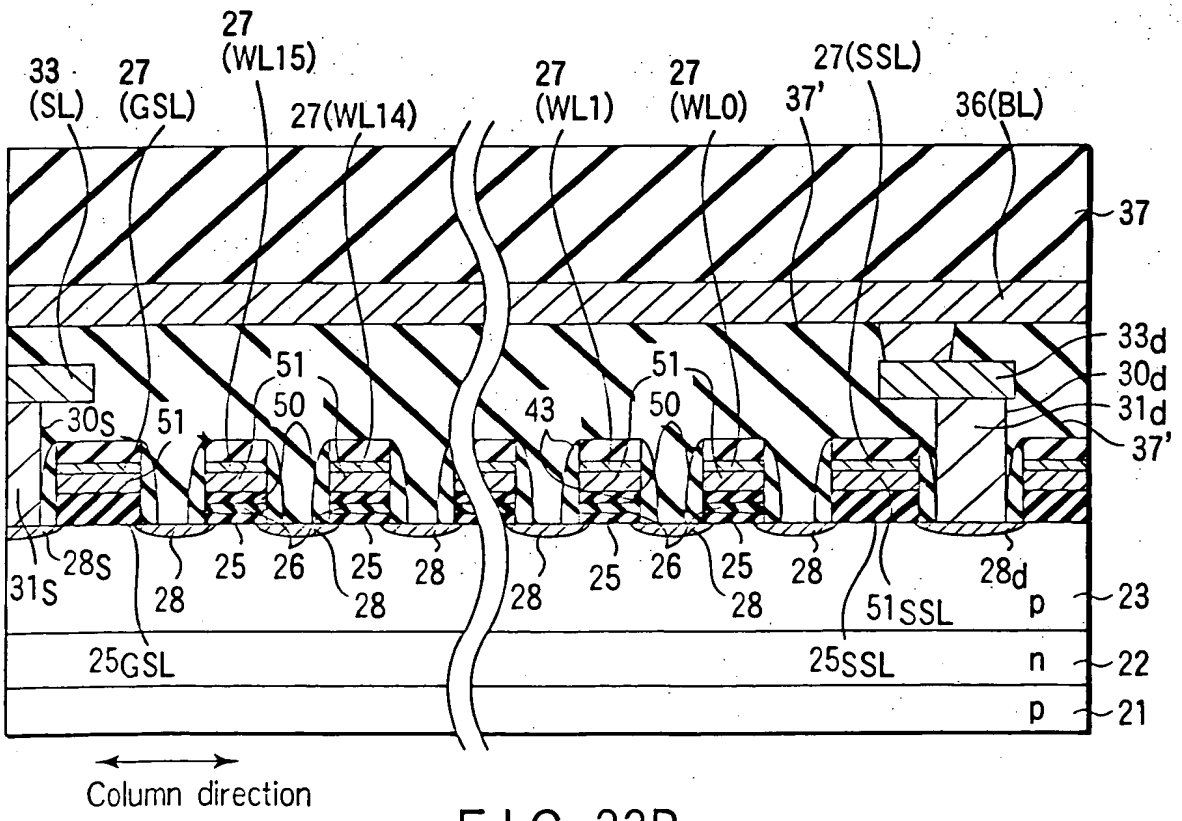

FIG. 33B

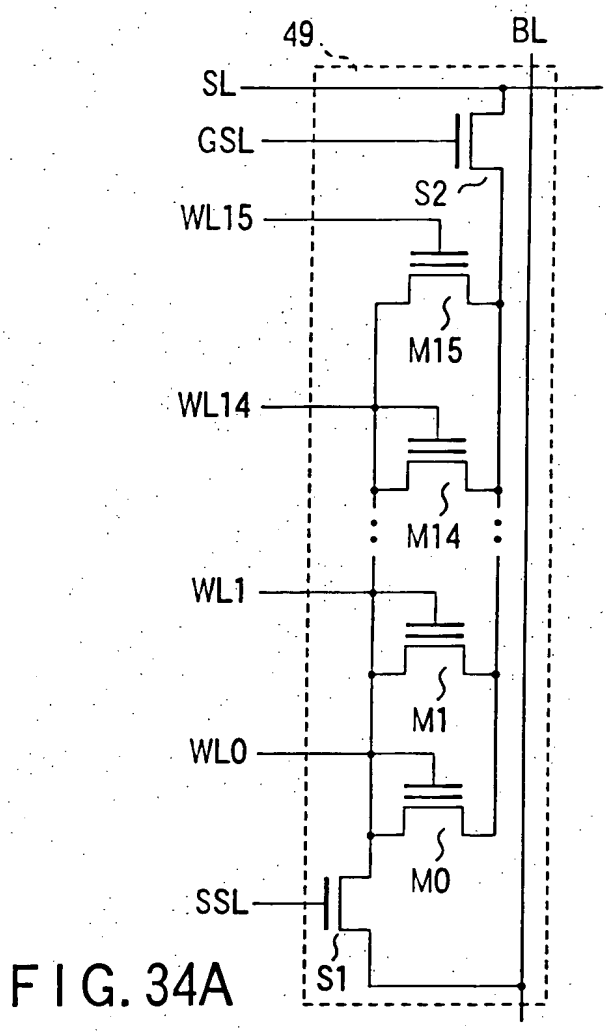

FIG. 34A

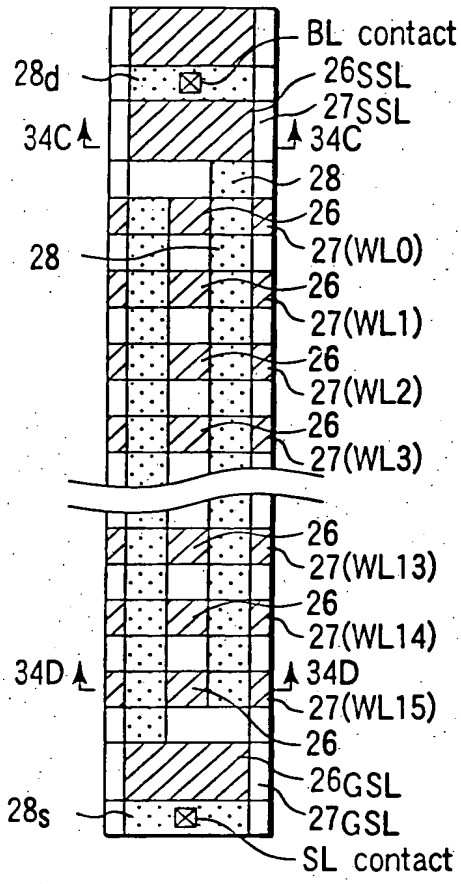

FIG. 34B

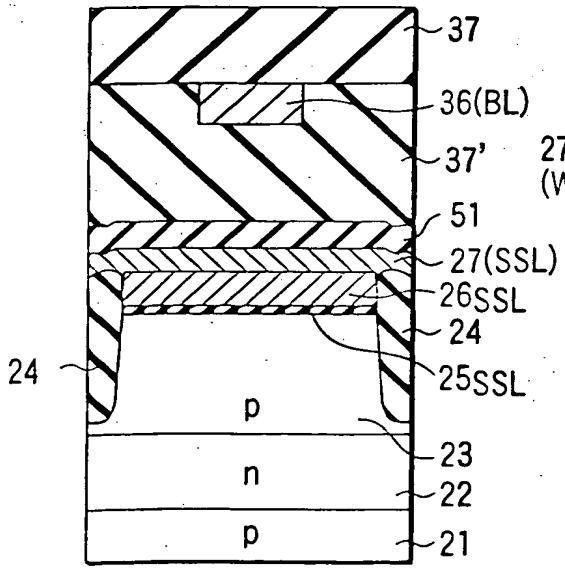

FIG. 34C

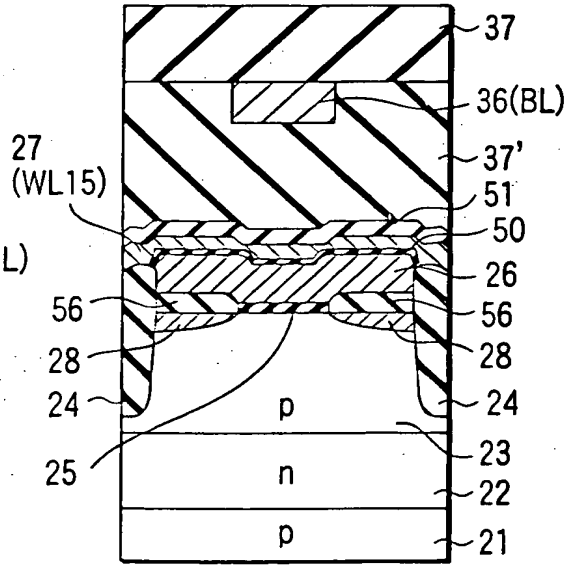

FIG. 34D

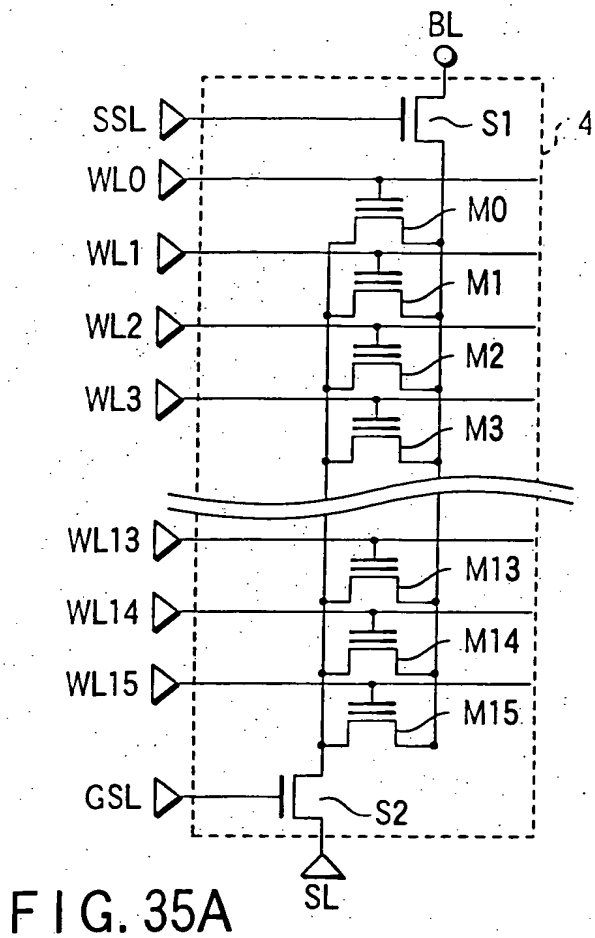

FIG. 35A

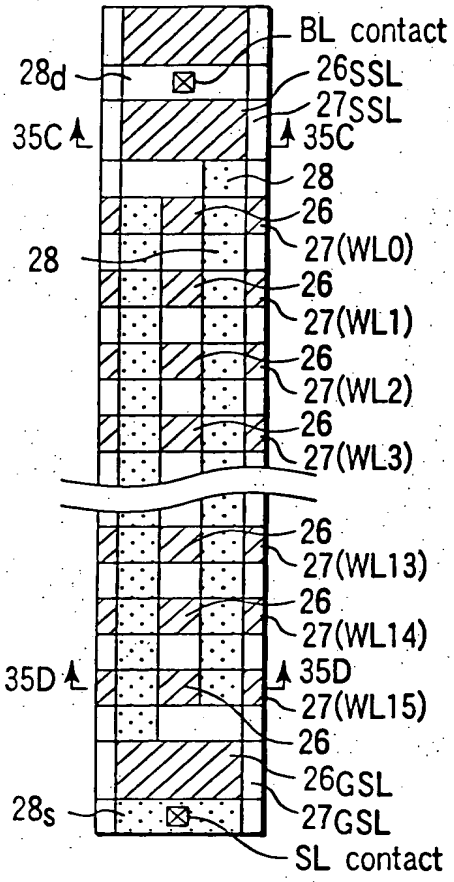

FIG. 35B

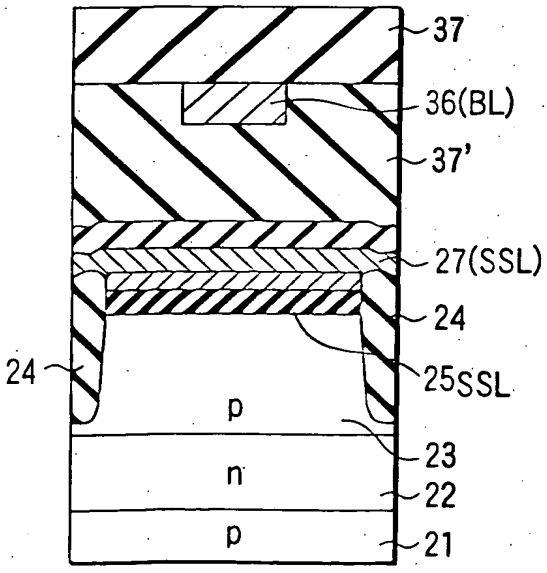

FIG. 35C

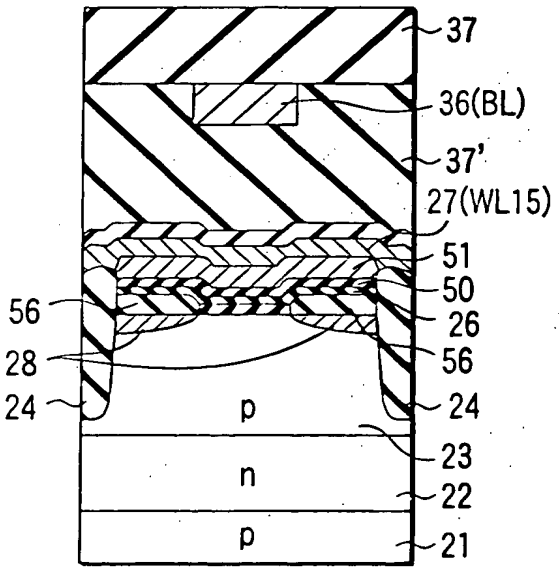

FIG. 35D

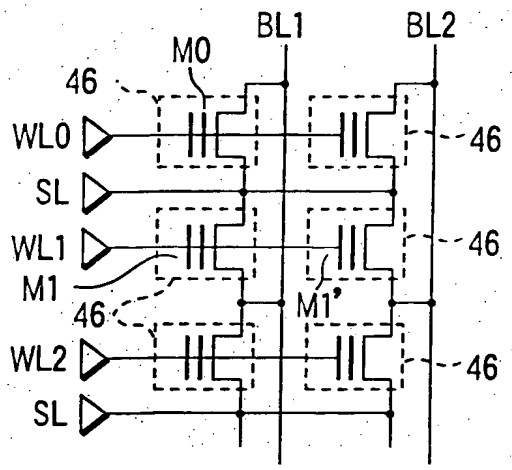

FIG. 36A

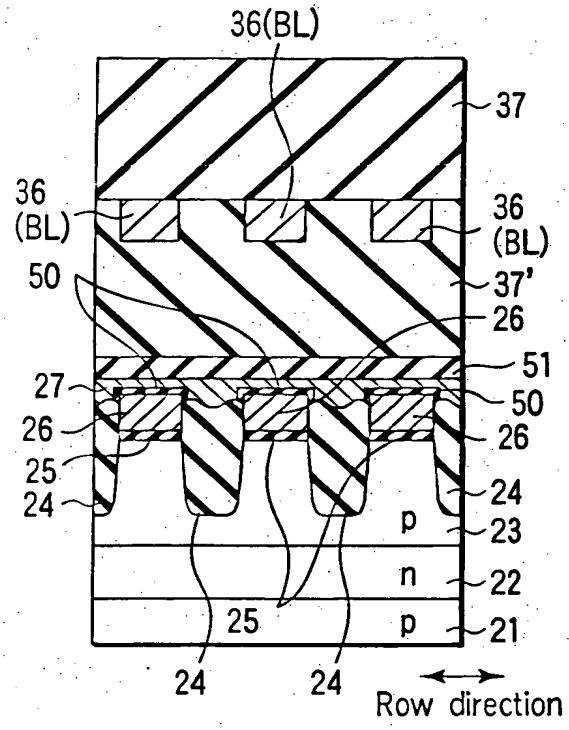

FIG. 36C

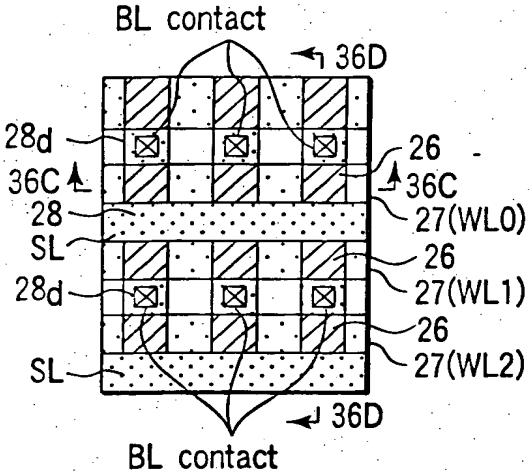

FIG. 36B

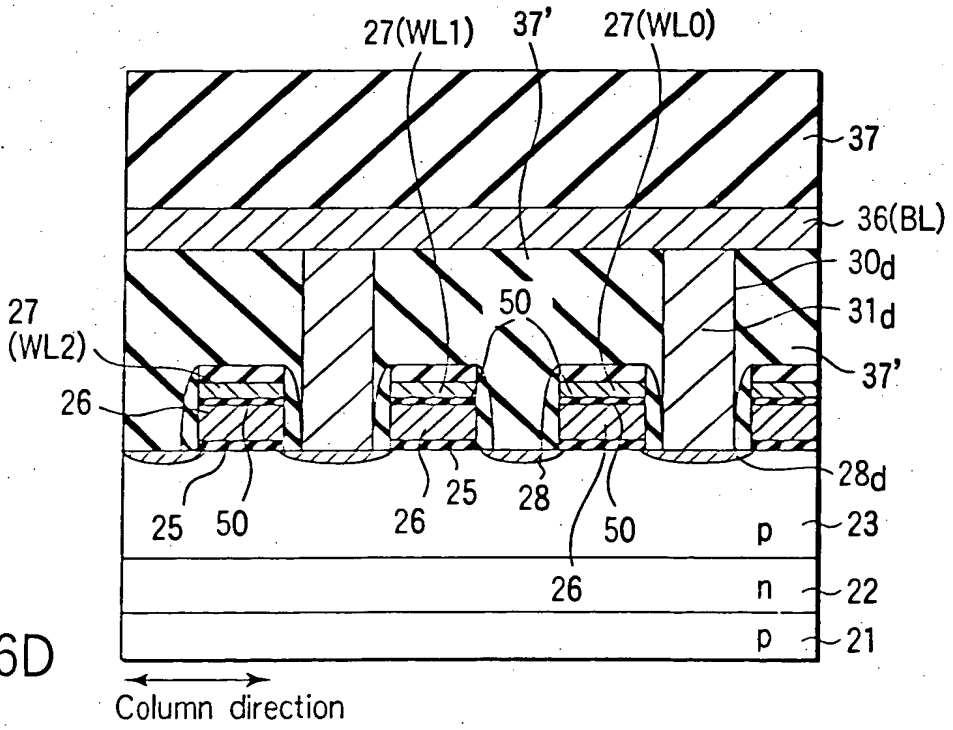

FIG. 36D

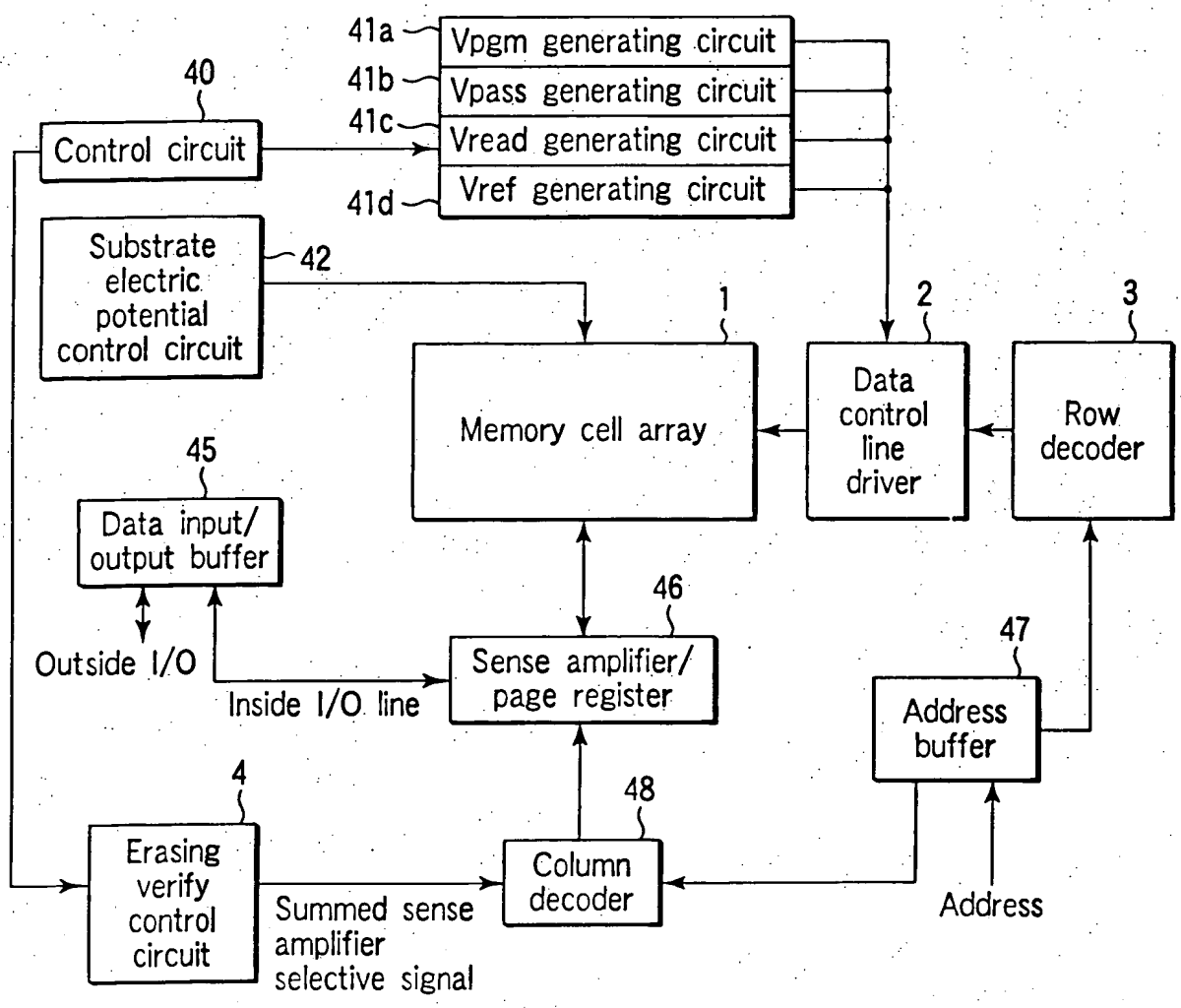

FIG. 37 PRIOR ART

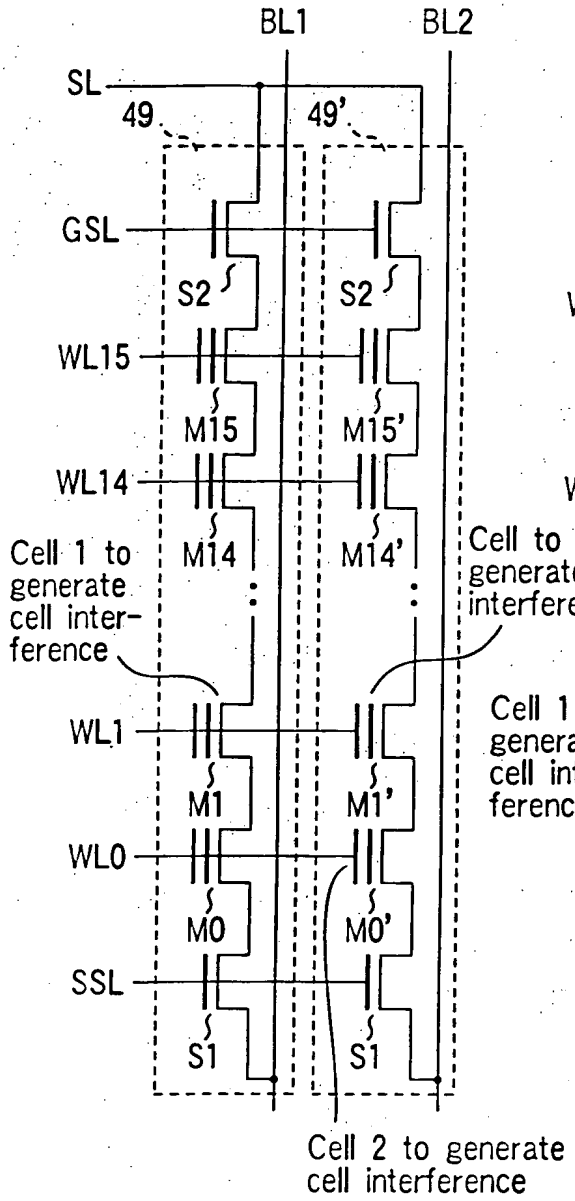

FIG. 38A
PRIOR ART

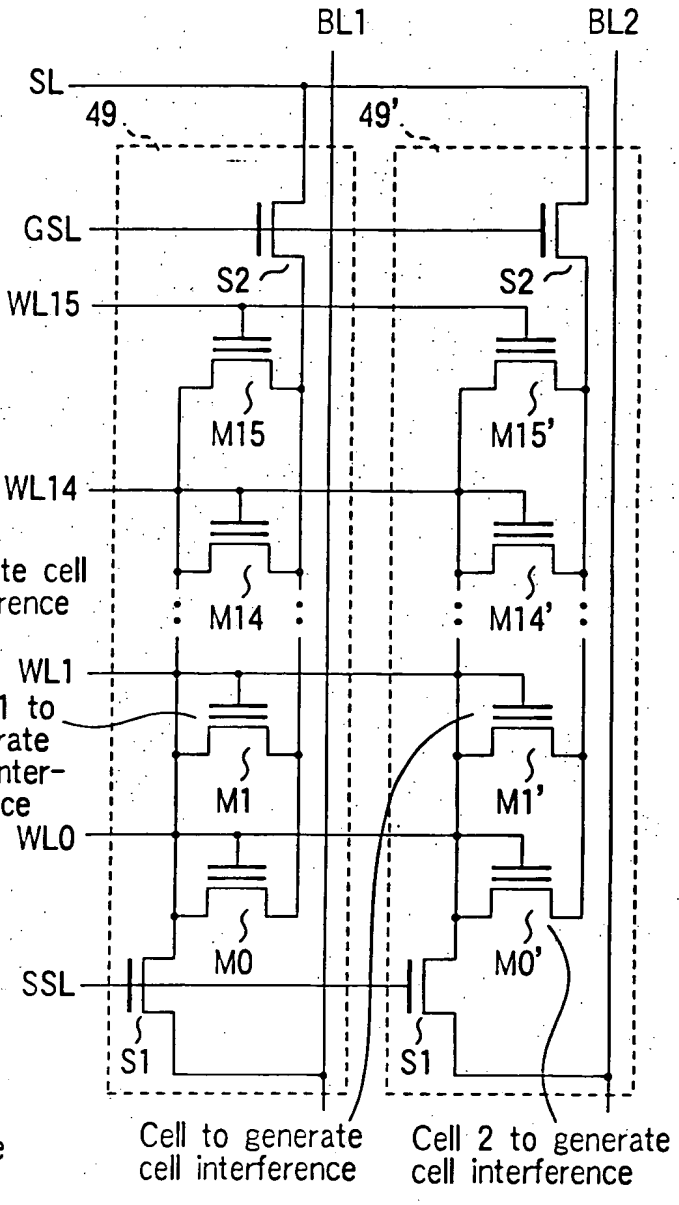

FIG. 38B
PRIOR ART

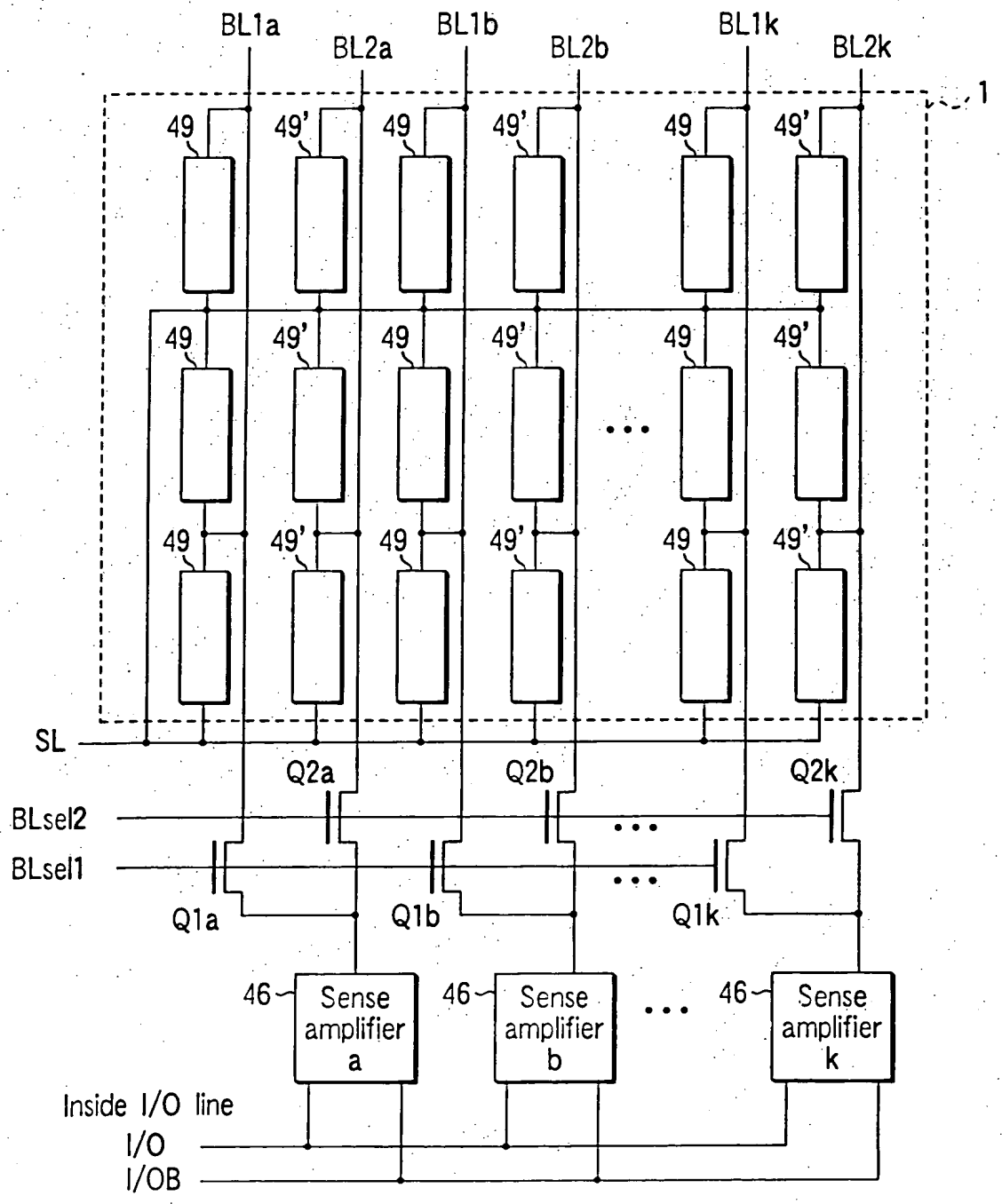

FIG. 39 PRIOR ART

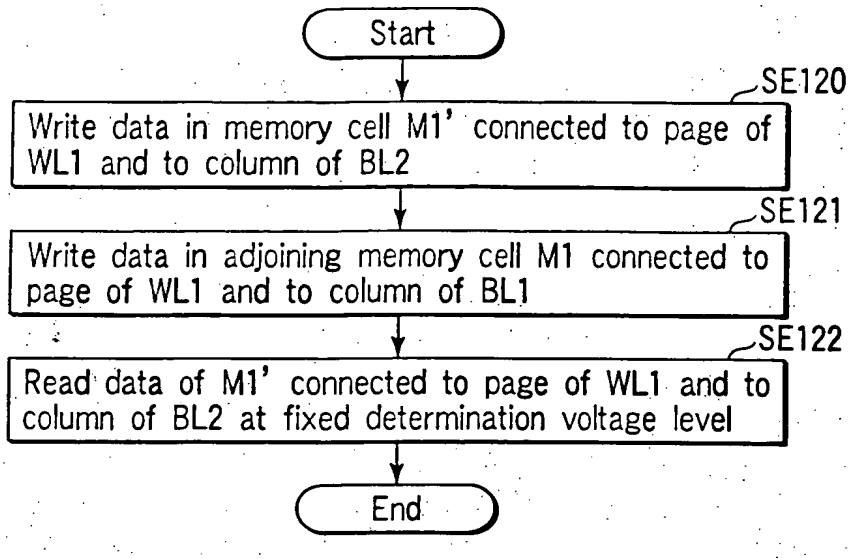

FIG. 40 PRIOR ART

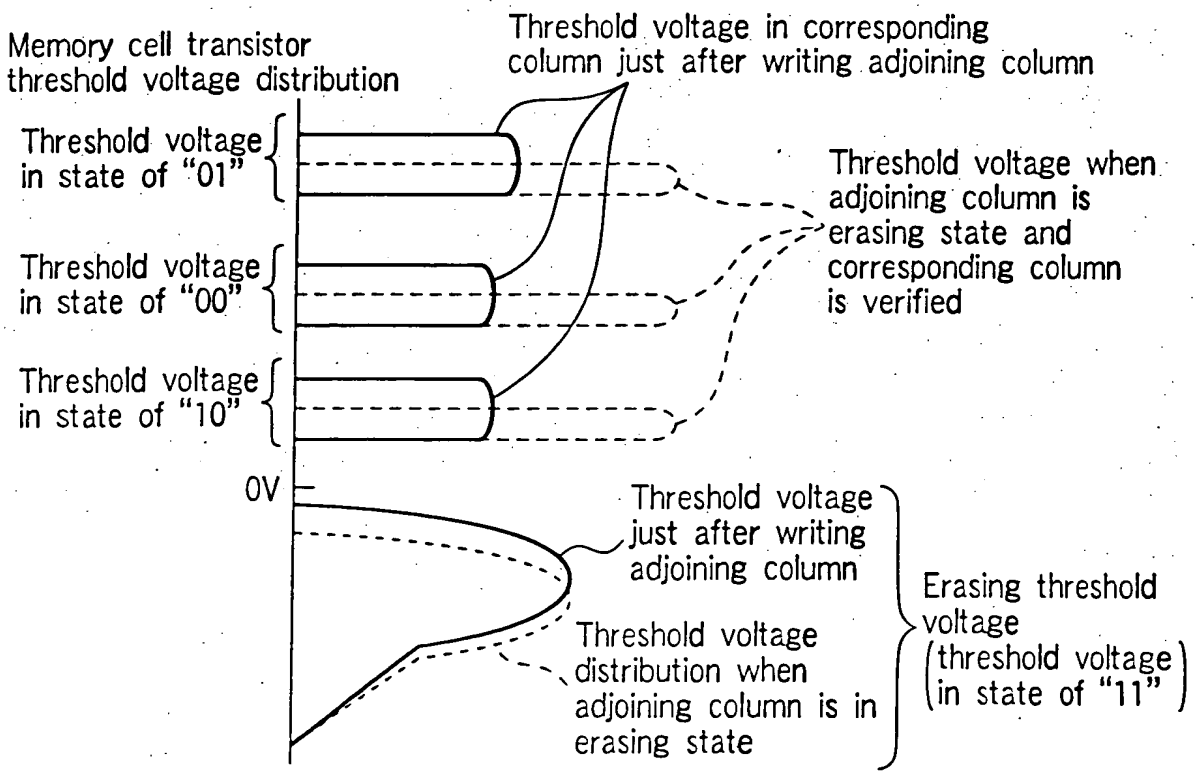

FIG. 41 PRIOR ART

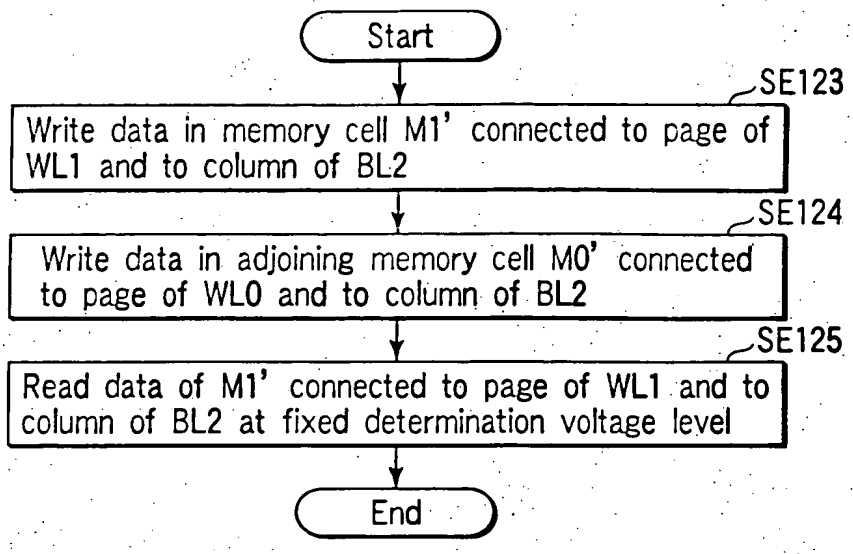

FIG. 42 PRIOR ART

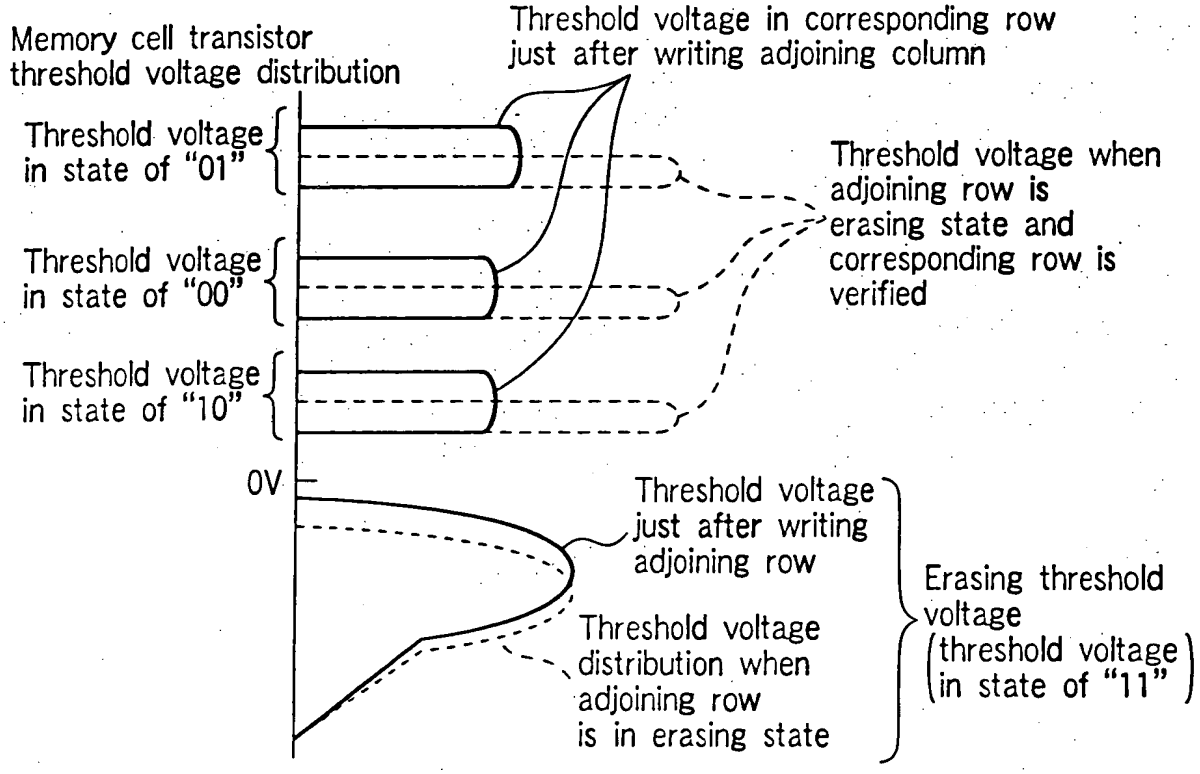

FIG. 43 PRIOR ART